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FUSION

(MS-7702L2 Ver:0A) mATX: 244mm * 244mm

CPU:

AMD FM1(Llano uPGA FAMILIES)

System Chipset:

AMD - Hudson D3/D2

On Board Chipset:

CLOCK GEN --FCH internal clock gen

LPC Super I/O --NCT6776F

LAN-Realtek 8111E/8105E

Azalia CODEC - Realtek ALC892/662/888/

Main Memory:

DDR III * 4 (max 32G)

Expansion Slots:

PCI Express X16 Slot * 1

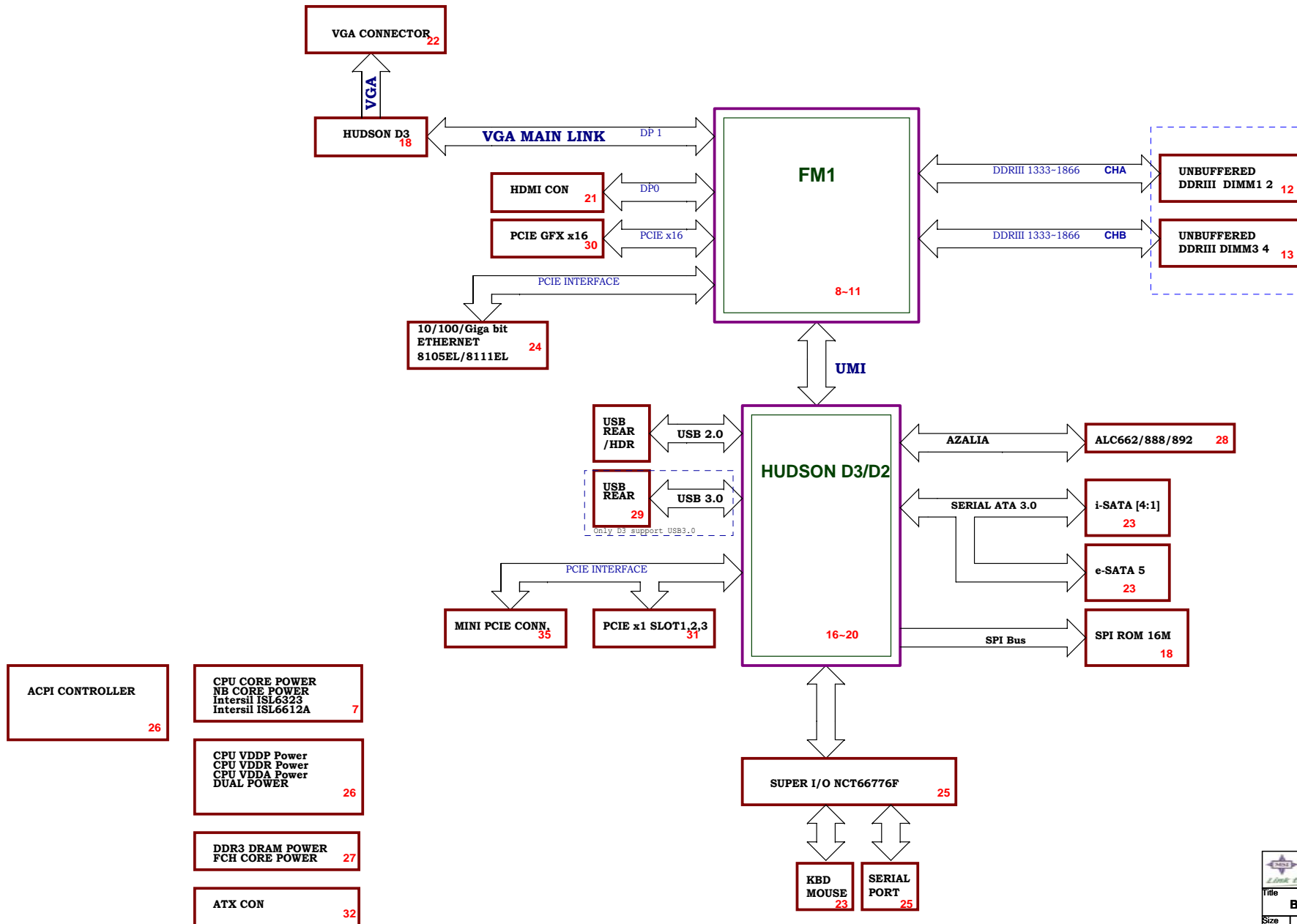
PCI Express X1 Slot * 3

MINI PCIE CONNECTOR *1

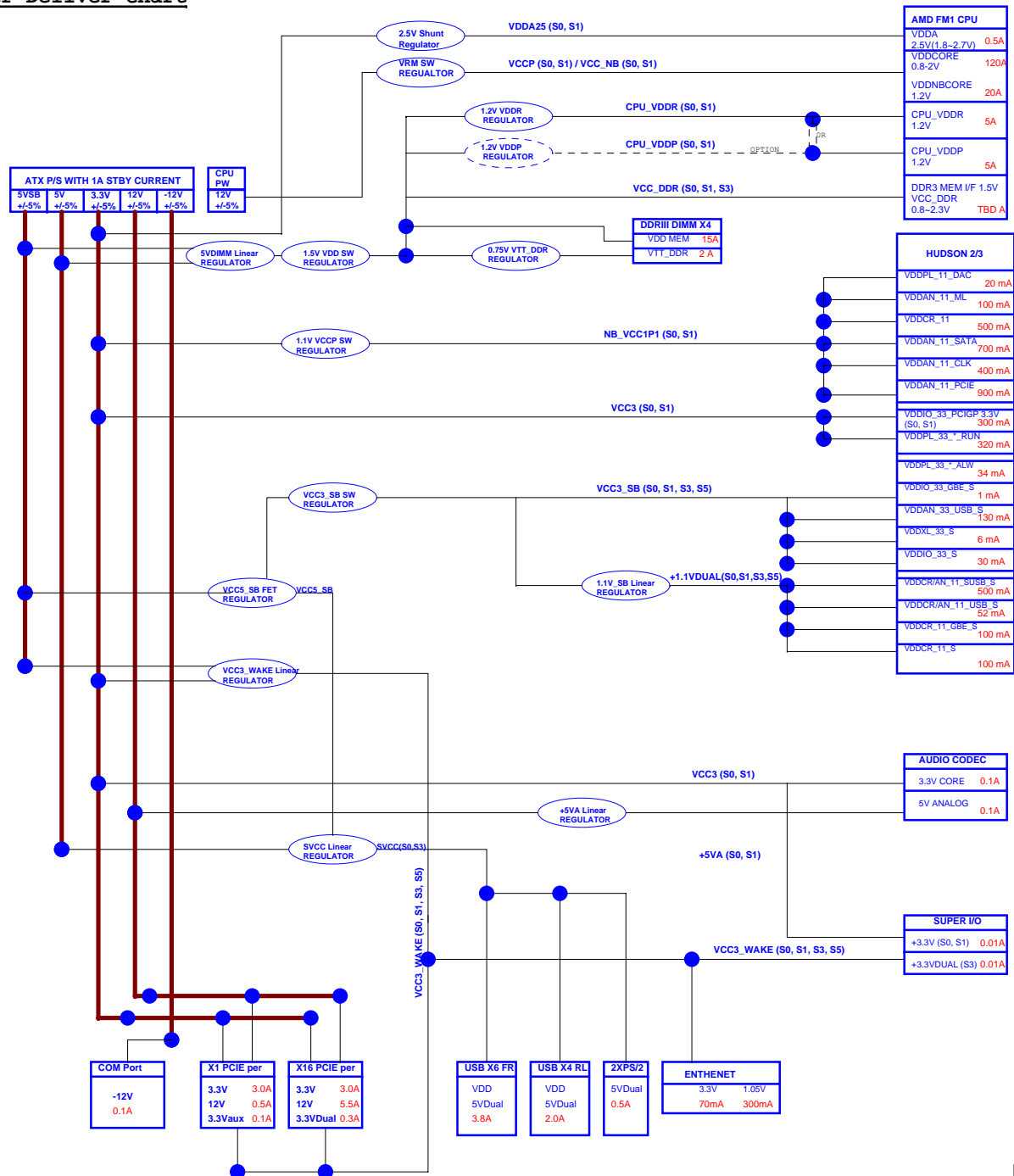
VRM

Controller - Intersil 6328 3+1 Phase

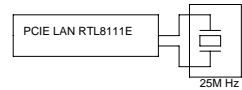
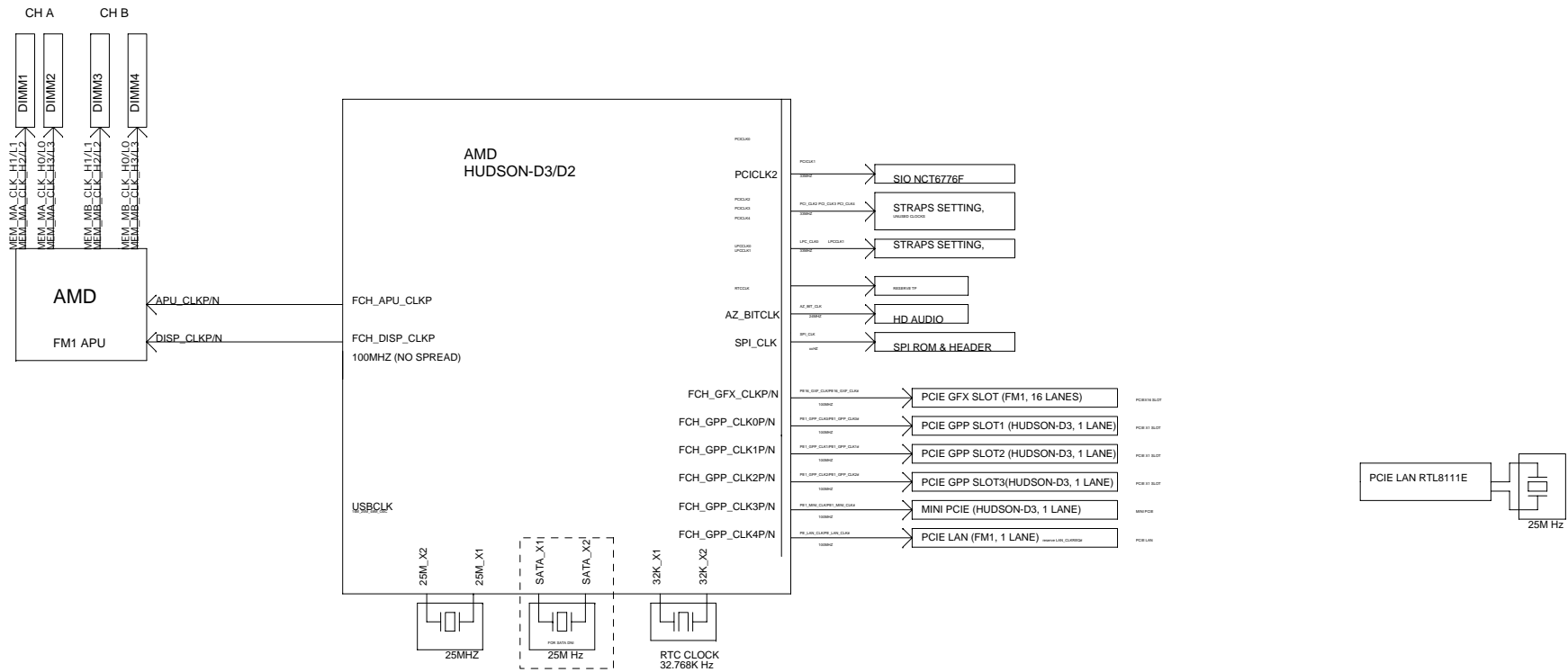
FUSION BLOCK DIAGRAM



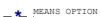
Power Deliver Chart



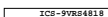
INTERNAL CLOCK MODE



PWRGD MAP



RESET MAP



POWER ON SEQUENCE



SIO NCT6776F GPIO Config

Pin	GPIO	Power Rail	Function description	Comment
38	GP46	VSB	SIO_WAKE	
39	YLV_LED/GP45	VSB	SUS_LED	reserved
40	GRN_LED/GP44	VSB	PWR_LED	
42	GP67	VSB	USB_EN	OD
44	GP65	VSB	MB_ID0	GPI reserved
45	GP64	VSB	MB_ID1	GPI reserved
47	GP63	VSB	MB_ID2	GPI reserved
48	GP62	VSB	COM_GPIO2	GPI
49	GP61	VSB	CHASSIS_ID1	GPI reserved
50	GP60	VSB	CHASSIS_ID2	GPI reserved
78	GP36	VSB	SIO_VDUAL_EN	

FCH HUDSON D3/D2GPIO Config

Pin	pin Name	Function description
AJ3	AD0/GPIO0	CLEAR_CMOS
J2	IR_LED#/LLB#/GPIO184	MINI_PWRON
AD22	SATA_ACT#/GPIO67	SATA_LED#:SATA Channel Active
M6	TEMPIN3/TALERT#/GPIO174	FCH_TALERT#:Thermal Alert. The FCH can be programmed to generate an SMI, SCI, or IRQ13 through GPE, or generate an SMI without GPE in response to the signal's assertion.
V3	SPI_CLK/GPIO162	SPI Clock
V6	SPI_DI/GPIO164	SPI Data In
V5	SPI_DO/GPIO163	SPI Data Output
T6	SPI_CS1#/GPIO165	SPI Chip Select1#
V1	ROM_RST#/SPI_WP#/GPIO161	SPI write protect (active low)
Y6	SPI_HOLD#/GEVENT9#	SPI HOLD#. Assert low to hold the SPI transaction.
T8	USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12#	OC#0:USB 3.0 port 3,USB 2.0 port 13
J7	USB_OC1#/TDI/GEVENT13#	OC#1:USB2.0 port 4,5
P5	USB_OC2#/TCK/GEVENT14#	OC#2:USB2.0 port 8,9
P5	USB_OC3#/AC_PRES/TDO/GEVENT15#	OC#3:USB 3.0 port 0,USB 2.0 port 10
P6	USB_OC4#/IR_RX0/GEVENT16#	OC#4:USB 3.0 port 1,USB 2.0 port 11
T1	USB_OC5#/IR_TX0/GEVENT17#	OC#5:USB2.0 port 2,3
R8	USB_OC6#/IR_TX1/GEVENT6#	OC#6:USB2.0 port 0,1
M7	BLINK/USB_OC7#/GEVENT18#	OC#7:USB 3.0 port 2,USB 2.0 port12
	GPIO[171::173];GPIO[175::182];GPIO[193::194]	Configure as one of the following: 10-kΩ 5% pull-up resistor to +3.3V_S5. 10-kΩ 5% pull-down resistor.

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1 CH-A	10100000B A0H	MEM_MA_CLK_H1/L1 MEM_MA_CLK_H2/L2
DIMM 2 CH-A	10100010B A4H	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H3/L3
DIMM 3 CH-B	10100001B A2H	MEM_MB_CLK_H1/L1 MEM_MB_CLK_H2/L2
DIMM 4 CH-B	10100011B A6H	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H3/L3

SMBus TABLE

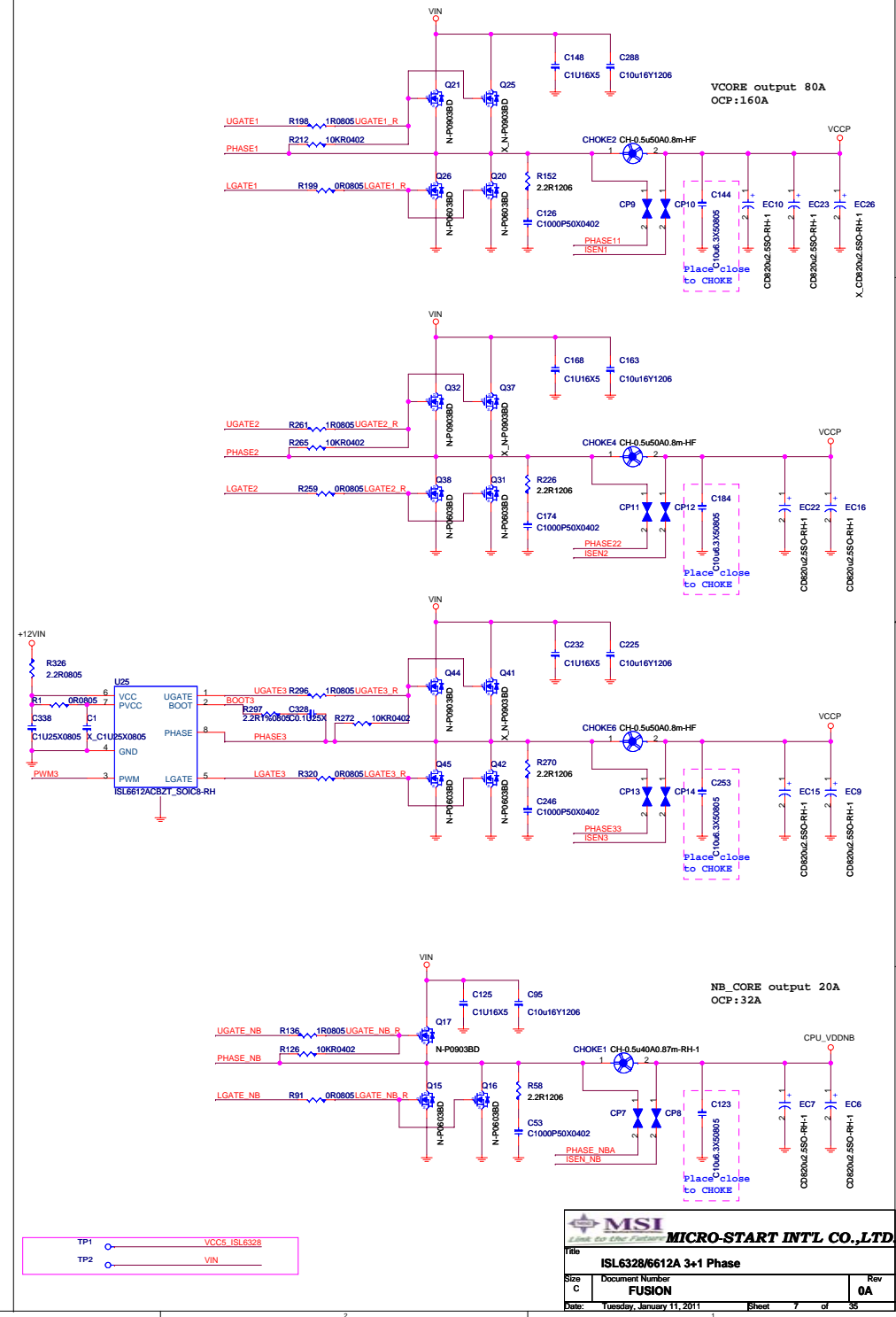
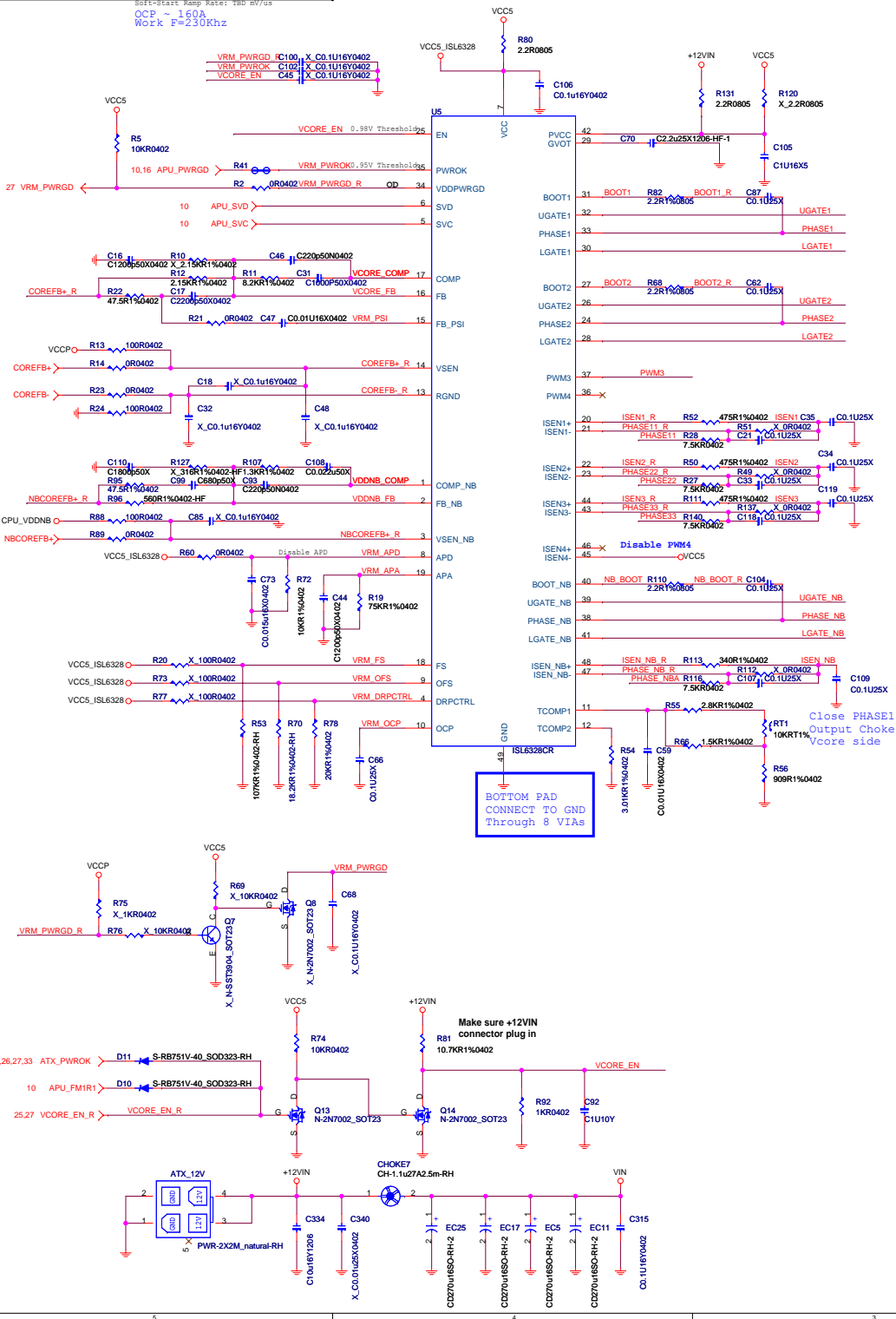
SOURCE	SINGLE NAME	LINKED DEVICE
APU	DPO_AUXP_C /DPO_AUXN_C	HDMI
	DP1_AUXP_C /DP1_AUXN_C	Hudson D2/3 DP to VGA translator
FCH	SCLK0/SDATA0	DIMMs,CLOCK GEN ,SIO
	SCLK1/SDATA1	LAN,PCIE SLOTS,MINI_PCIE
	SCLK3/SDATA3	TP

RESET TABLE

SOURCE	SINGLE NAME	LINKED DEVICE
FCH	PCIE_RST#	PCie 16X,1X,LAN,MINI_PCIE
	A_RST#	SIO,LPC debug
	PCIE_RST2#	RESERVE TP
	LDT_RST#	APU
	AZ_RST#	AZALIA CODEC
	DDR3_RST#	NC
	FC_RST#	DEBUG BUS
	ROM_RST#	NC
FRONT PANEL	FP_RST#	FCH,CLOCK GEN

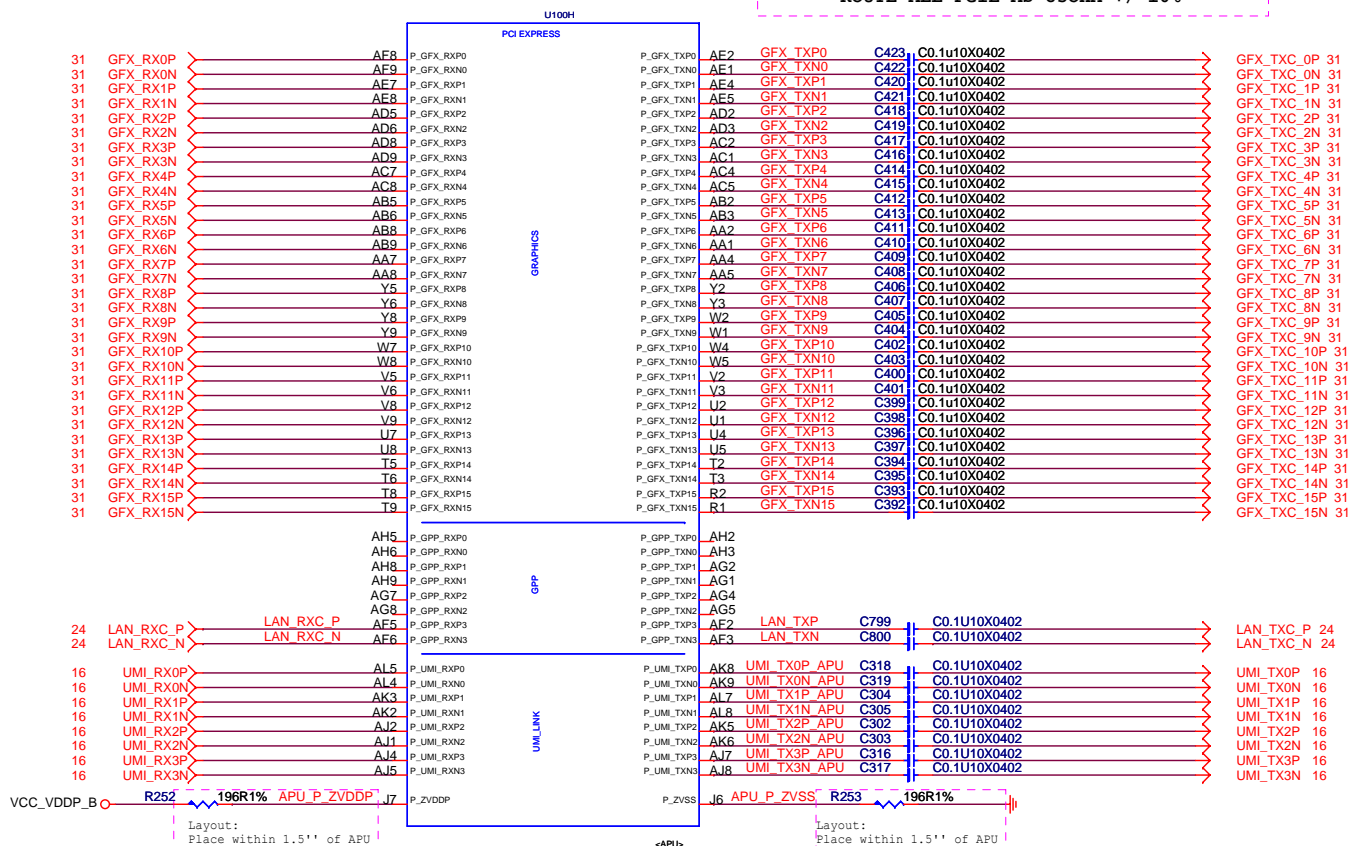
ISL6328/6612A 3+1 Phase

Soft-Start Ramp Rate: TBD mV/us
OCP ~ 160A
Work F=230Khz



FM1 PCIE I/F

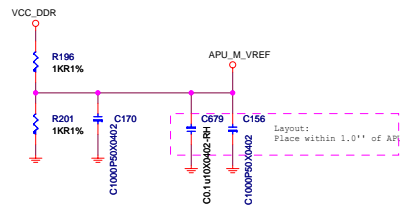
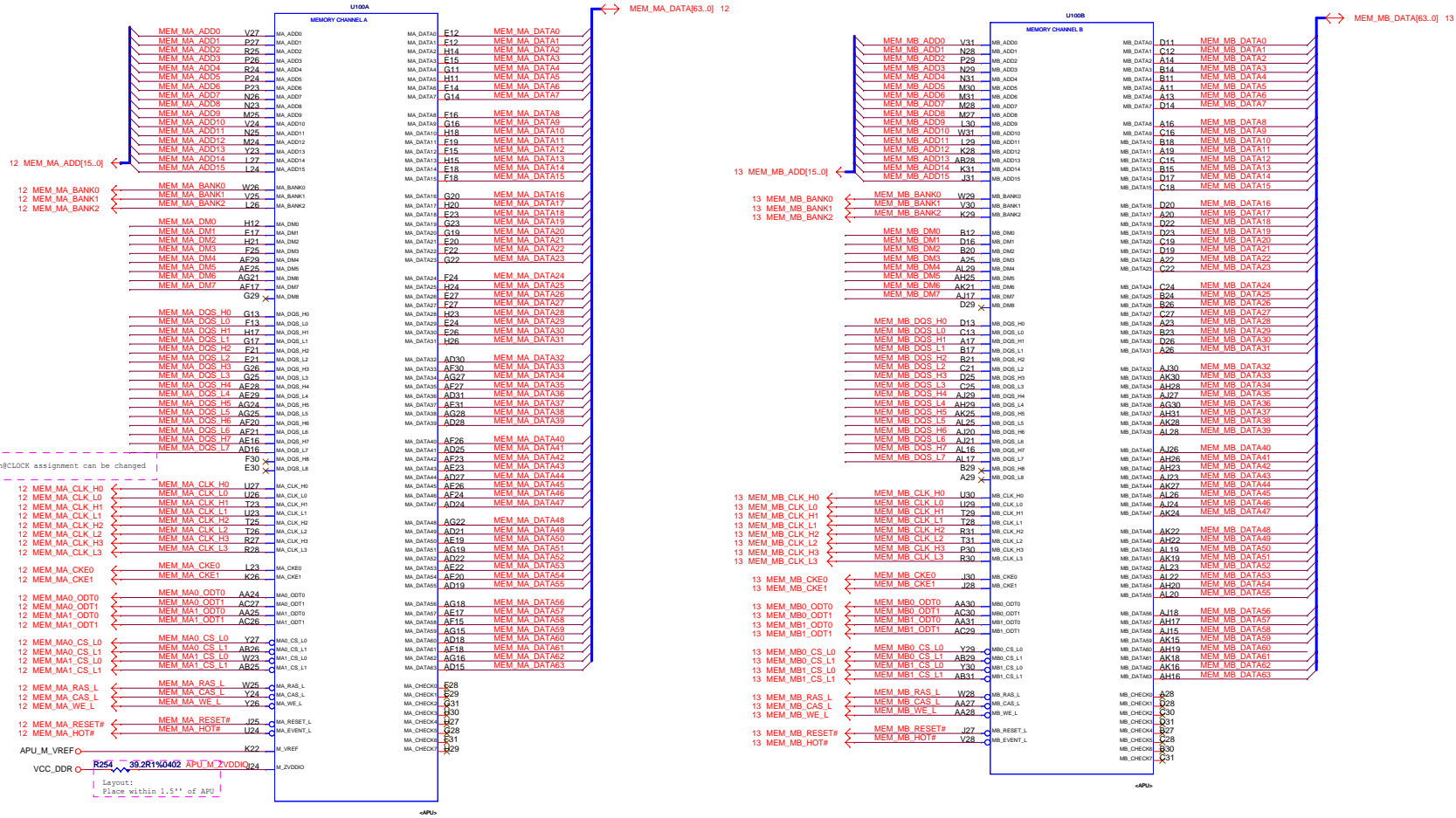
mach@CRB PCIE AC Capacitors:75nF to 200nF
Layout: PLACE CAPS WITH APU < 1 INCH
ROUTE ALL PCIE AS 850HM +/-10%



FM1DDR3 I/F

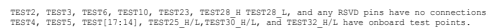
12 MEM_MA_DQS_L[7..0] ←→
12 MEM_MA_DQS_H[7..0] ←→
12 MEM_MA_DM[7..0] ←→

13 MEM_MB_DQS_L[7..0] ←→
13 MEM_MB_DQS_H[7..0] ←→
13 MEM_MB_DM[7..0] ←→



Note: Several vias on the DPO interface violate the minimum distance rules for via to via spacing between diff pairs. These violations have been reviewed and approved on an individual basis, and pose no significant signal integrity issues for this implementation since the route lengths are under the maximum allowed spec, and the via distance violations are not severe.

U100C
ANALOG/DISPLAY/MISC
DP0_TXP0
DP0_TXN0
DP_AUX_ZVSS
R207 150R1%0402
Layout: Place within 1.5" of APU



VCC_D0R

R307 1KR0402 APU_SIC_R

R317 1KR0402 APU_SID

R288 300R0402 APU_RST#

R310 300R0402 APU_PWRGD

R289 300R0402 APU_PROCHOT#

R290 300R0402 APU_ALG1#

R290 1KR0402 APU_THERMTRIP#

R318 1KR0402 FCH_DMA_ACTIVE#

R301 10KR0402 APU_FMR1#

VCC5_SB

To override VID: remove R520, R521
 Stuff R62 to enter FIX mode

		R520 Voltage	
SVC	SVD	Pre-PBANK metal	VID
0	0	0.0	1.0
0	1	0.0	1.1
1	0	0.0	1.2
1	1	0.0	1.3
0	0	0.1	1.4
0	1	0.1	1.5
1	0	0.1	1.6
1	1	0.1	1.7
0	0	0.2	1.8
0	1	0.2	1.9
1	0	0.2	2.0
1	1	0.2	2.1
0	0	0.3	2.2
0	1	0.3	2.3
1	0	0.3	2.4
1	1	0.3	2.5
0	0	0.4	2.6
0	1	0.4	2.7
1	0	0.4	2.8
1	1	0.4	2.9
0	0	0.5	3.0
0	1	0.5	3.1
1	0	0.5	3.2
1	1	0.5	3.3
0	0	0.6	3.4
0	1	0.6	3.5
1	0	0.6	3.6
1	1	0.6	3.7
0	0	0.7	3.8
0	1	0.7	3.9
1	0	0.7	4.0
1	1	0.7	4.1
0	0	0.8	4.2
0	1	0.8	4.3
1	0	0.8	4.4
1	1	0.8	4.5
0	0	0.9	4.6
0	1	0.9	4.7
1	0	0.9	4.8
1	1	0.9	4.9
0	0	1.0	5.0
0	1	1.0	5.1
1	0	1.0	5.2
1	1	1.0	5.3
0	0	1.1	5.4
0	1	1.1	5.5
1	0	1.1	5.6
1	1	1.1	5.7
0	0	1.2	5.8
0	1	1.2	5.9
1	0	1.2	6.0
1	1	1.2	6.1
0	0	1.3	6.2
0	1	1.3	6.3
1	0	1.3	6.4
1	1	1.3	6.5
0	0	1.4	6.6
0	1	1.4	6.7
1	0	1.4	6.8
1	1	1.4	6.9
0	0	1.5	7.0
0	1	1.5	7.1
1	0	1.5	7.2
1	1	1.5	7.3
0	0	1.6	7.4
0	1	1.6	7.5
1	0	1.6	7.6
1	1	1.6	7.7
0	0	1.7	7.8
0	1	1.7	7.9
1	0	1.7	8.0
1	1	1.7	8.1
0	0	1.8	8.2
0	1	1.8	8.3
1	0	1.8	8.4
1	1	1.8	8.5
0	0	1.9	8.6
0	1	1.9	8.7
1	0	1.9	8.8
1	1	1.9	8.9
0	0	2.0	9.0
0	1	2.0	9.1
1	0	2.0	9.2
1	1	2.0	9.3
0	0	2.1	9.4
0	1	2.1	9.5
1	0	2.1	9.6
1	1	2.1	9.7
0	0	2.2	9.8
0	1	2.2	9.9
1	0	2.2	10.0
1	1	2.2	10.1
0	0	2.3	10.2
0	1	2.3	10.3
1	0	2.3	10.4
1	1	2.3	10.5
0	0	2.4	10.6
0	1		

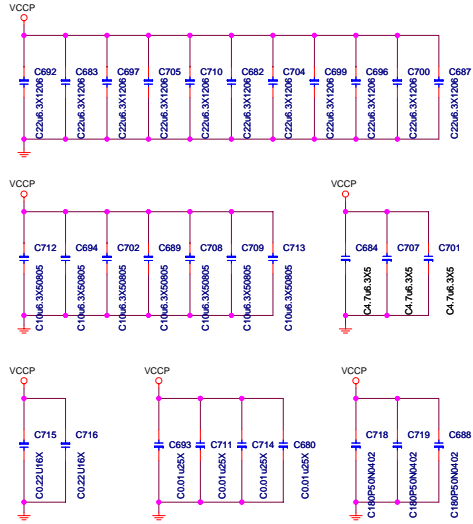


APU TEST18	TP46
APU TEST19	TP64
APU TEST21	TP65
APU TEST22	TP67
APU TEST12	TP68
APU TEST24	TP69
APU TEST20	TP70

APU_RST# TP71

APU TEST14	TF
APU TEST15	TF
APU TEST16	TF
APU TEST17	TF
APU BLON	TF
APU DIGON	TF
APU BLPWM	TF
DPI HPD VGA C	TF

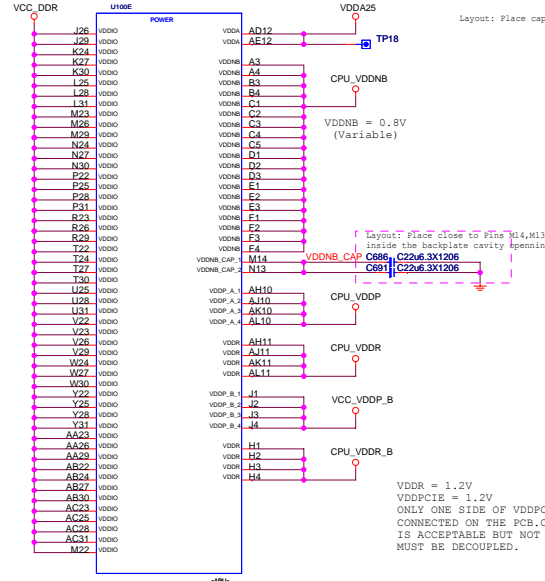
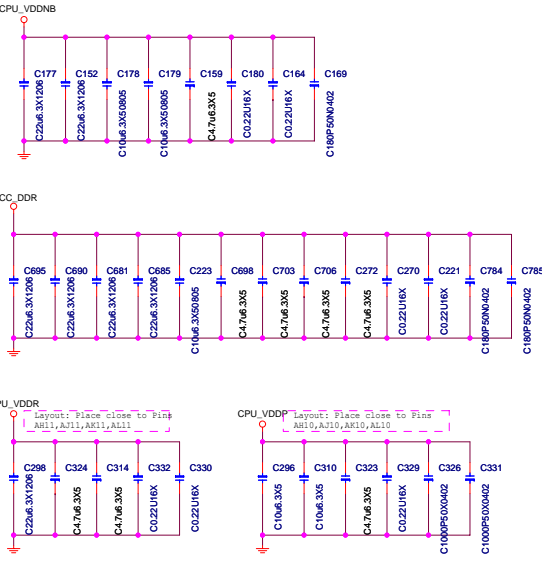
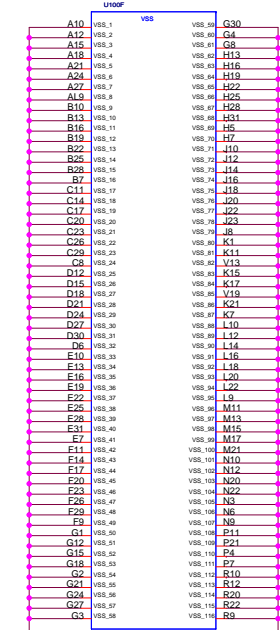
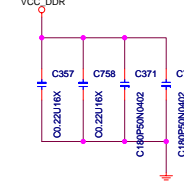
BOTTOM SIDE DECOUPLING



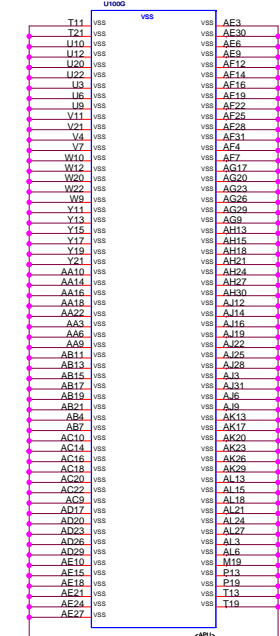
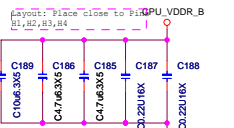
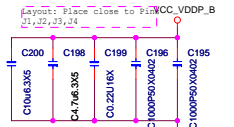
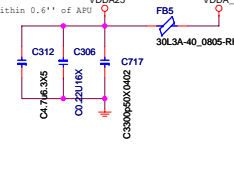
FM1 DECOUPLING CAPS

TOTLE POWER PINS	VSS	VDD	VDDNB	VDDIO	VDDP	VDDR	VDDA	Mvref
416	226	102	19	51	8	8	4	2
VALUE/SIZE/ MATERIAL	COMB	COMB	SPLIT	SPLIT				
220/1206/X5R	/	11	2	4	/	1	/	/
100/0805/X5R	/	7	2	1	2+1(B)	1	/	/
4.70/0805/X5R	/	3	1	4	2	2+2	2	1
0.22U/0603/X5R	/	2	2	2+2	2	2	2	1
0.10U/0603/X5R	/	/	/	/	/	/	/	1
0.01U/0603/X5R	/	4	/	/	/	/	/	/
3.3 nF/0603/X5R	/	/	/	/	/	/	/	1
1 nF/0603/X5R	/	/	/	/	/	/	/	1
1 nF/0603/X5R	/	/	/	/	4	/	/	/
180 pF/0603/X5R	/	3	1	2+2	2	/	/	/

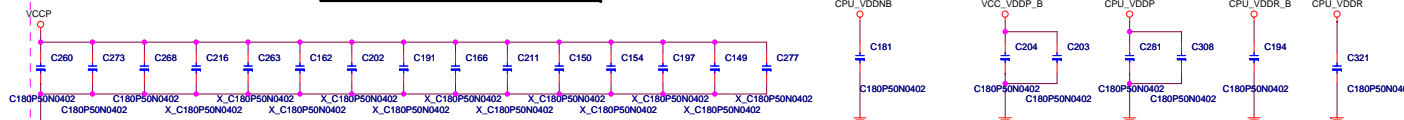
Place across each VDDIO-GND plane seam

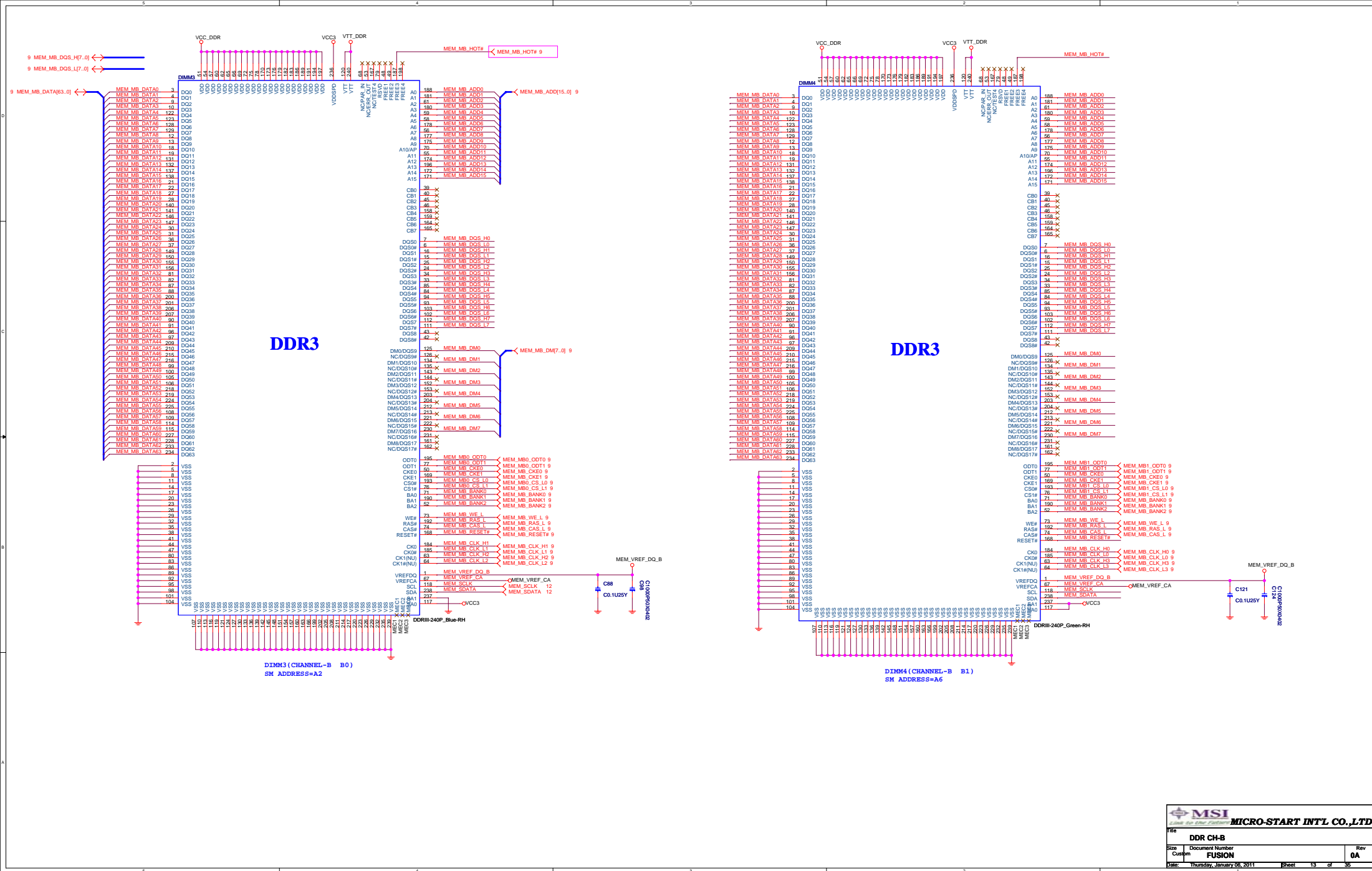


VDDR = 1.2V
VDDP/IE = 1.2V
ONLY ONE SIDE OF VDDPCIE & VDDR MUST BE CONNECTED TO THE PCB. CONNECTING BOTH SIDES IS ACCEPTABLE BUT NOT REQUIRED. BOTH SIDES MUST BE DECOUPLED.

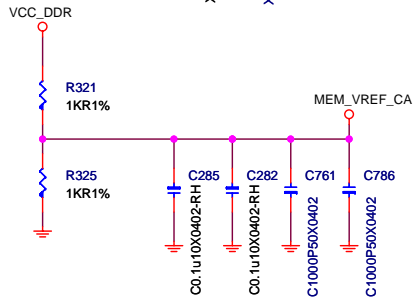
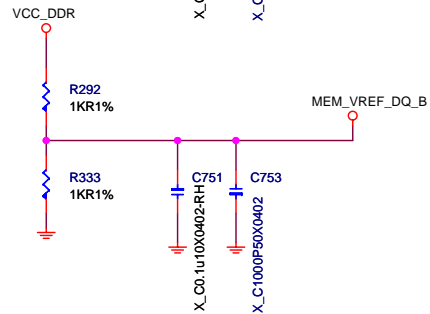
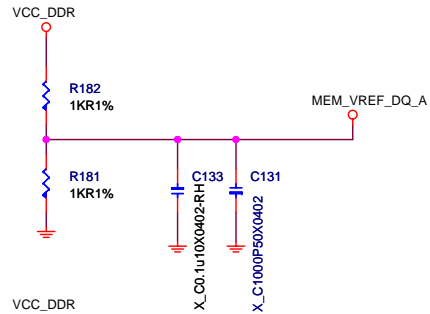


EMC Caps On Bottom side



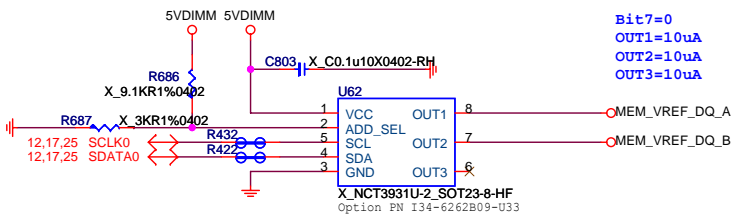


DDR REF POWER & CAPS



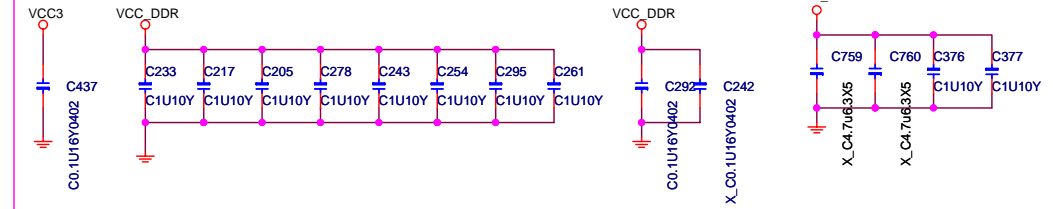
VOLTAGE CONSOLE

0x28:RH=9.1K,RL=3K;Bit7=0

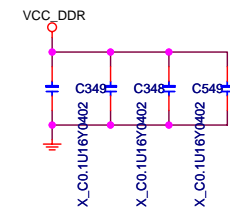
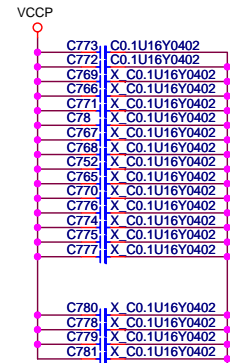
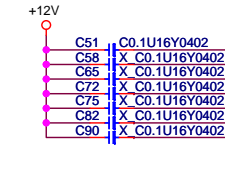
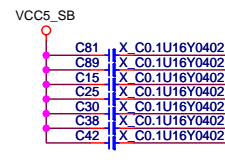
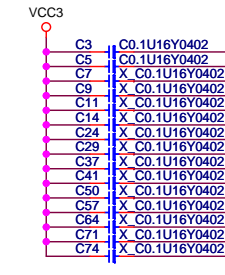
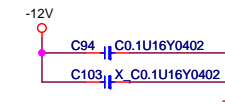
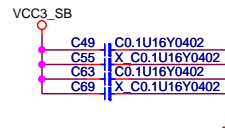
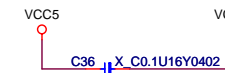
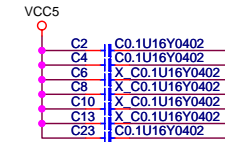


Bit7=0
OUT1=10uA
OUT2=10uA
OUT3=10uA

De-coupling Caps For DIMMs

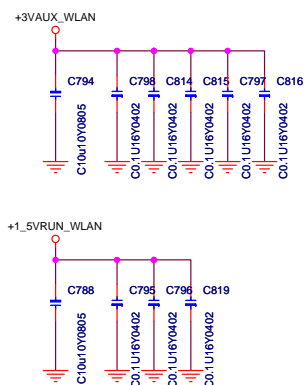
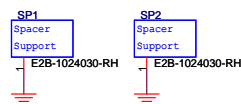
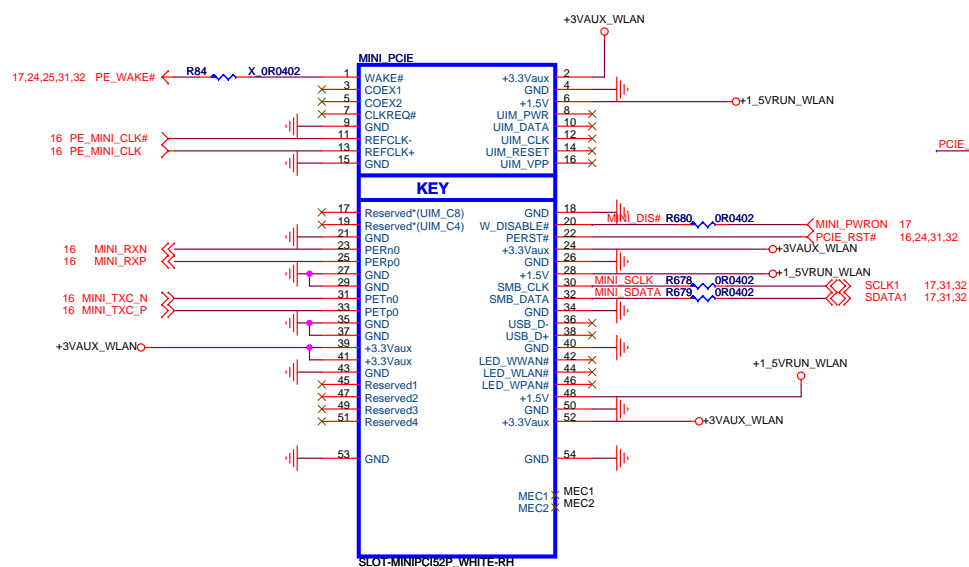


EMI Reserved

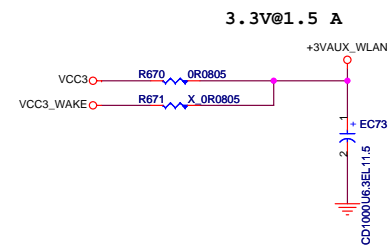
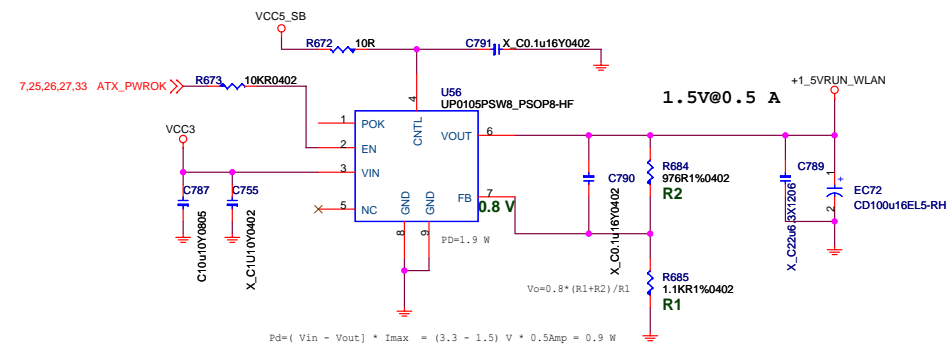


MICRO-START INT'L CO.,LTD.		
Title		
DDR REF POWER & CAPS		
Size B	Document Number	Rev
	FUSION	0A
Date:	Thursday, January 06, 2011	Sheet 14 of 35

MINI PCIE CONN,

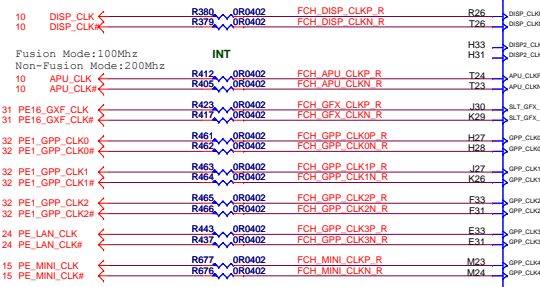
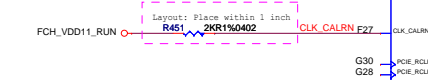
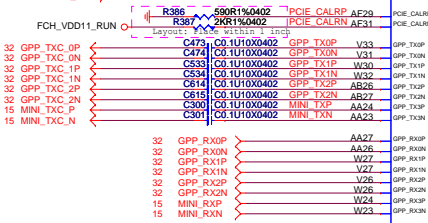
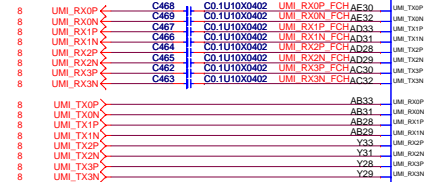
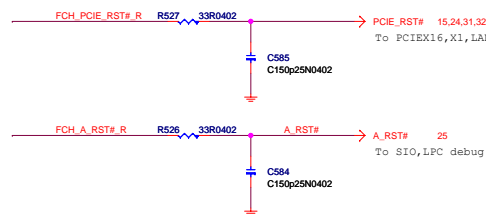


+1_5VRUN_WLAN POWER

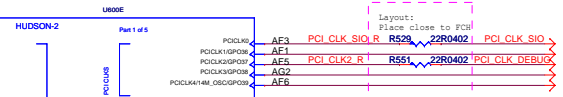
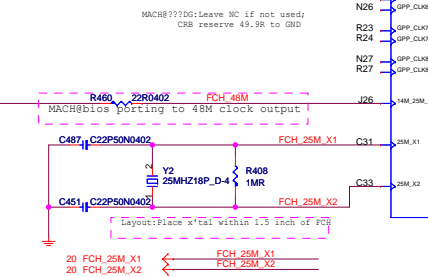
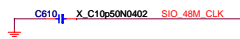


HUDSON PCIe/PCI/APU/LPC/CLK

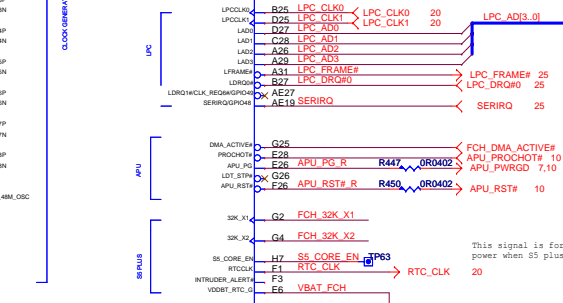
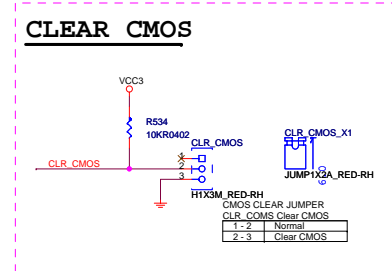
A RST# for LPC device;
PCIE_RST# for APU PCIE device;
PCIE_RST#2 FCH PCIE device



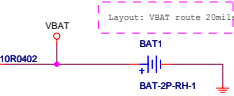
For external clock generator mode:
100-MHz reference clock for the FCH. Spreadcapable
For internal clock generator mode:
Not used. Left unconnected.
The function is selected by the pin strap "CLKGEN"
(pin LPCCLK1).



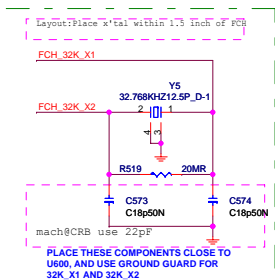
If PCI not implemented: Provide test points or other means to allow access for debug purposes use these balls for alternate GPIO/GPO functions or leave unconnected.



Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the APU I/O rail. They are also in the S5 domain to prevent glitching at power up.



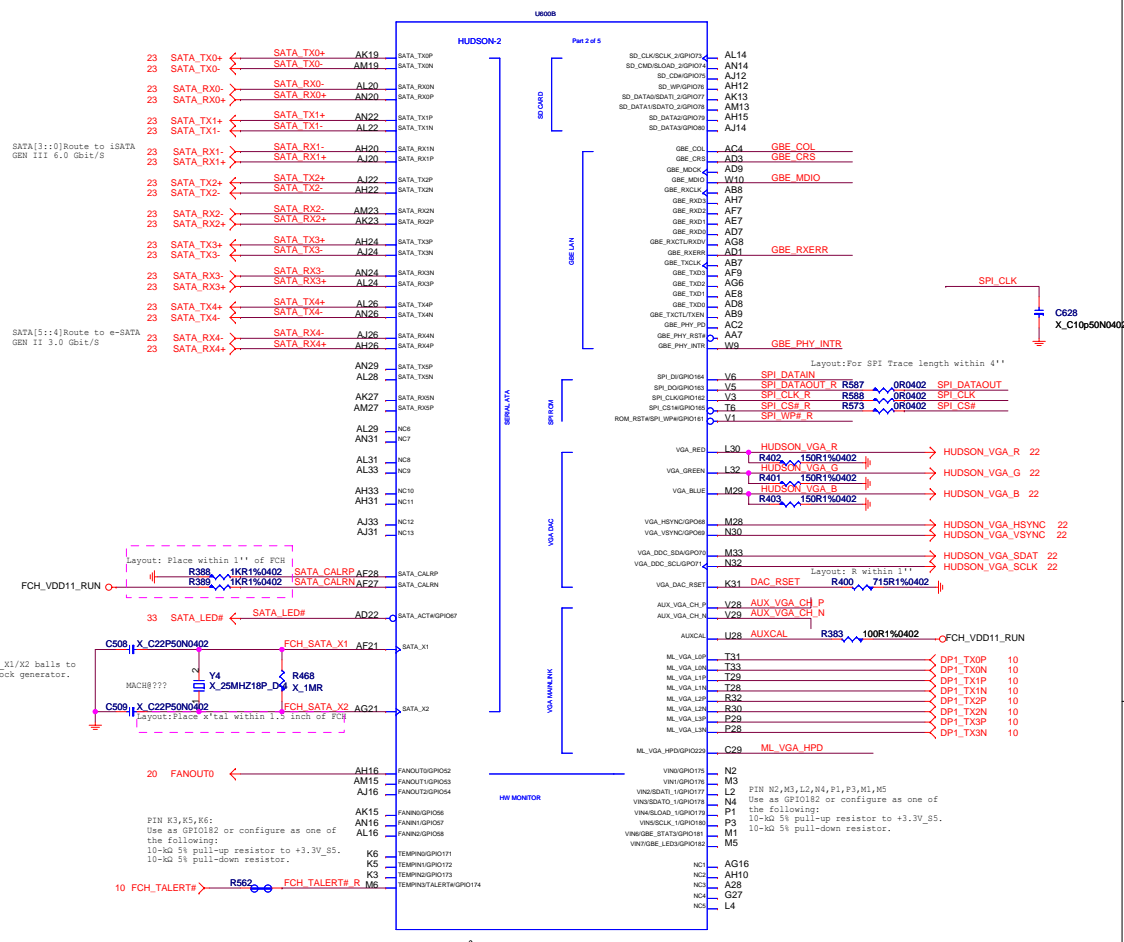
FCH 50KR internal PU to VBAT



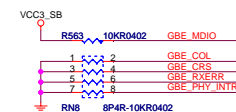
10

HUDSON SATA/VGA/SPI/HWM

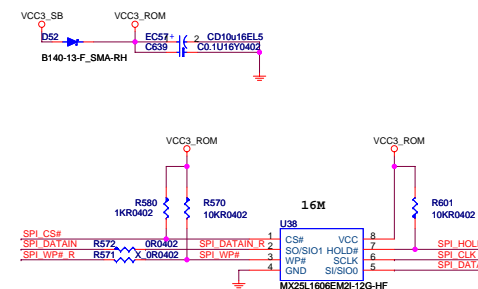
LAYOUT:
ROUTE SATA TX DIFF PAIR @ 100 OHM+/-10%
RX DIFF PAIR @ 90 OHM+/-10%



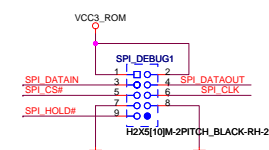
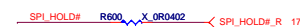
GBE NOT ENABLED



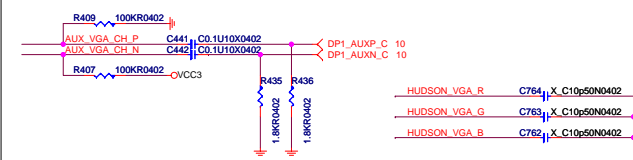
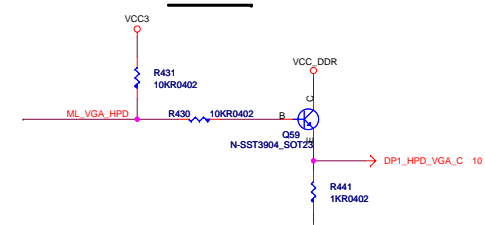
SPI ROM & DEBUG HEADER



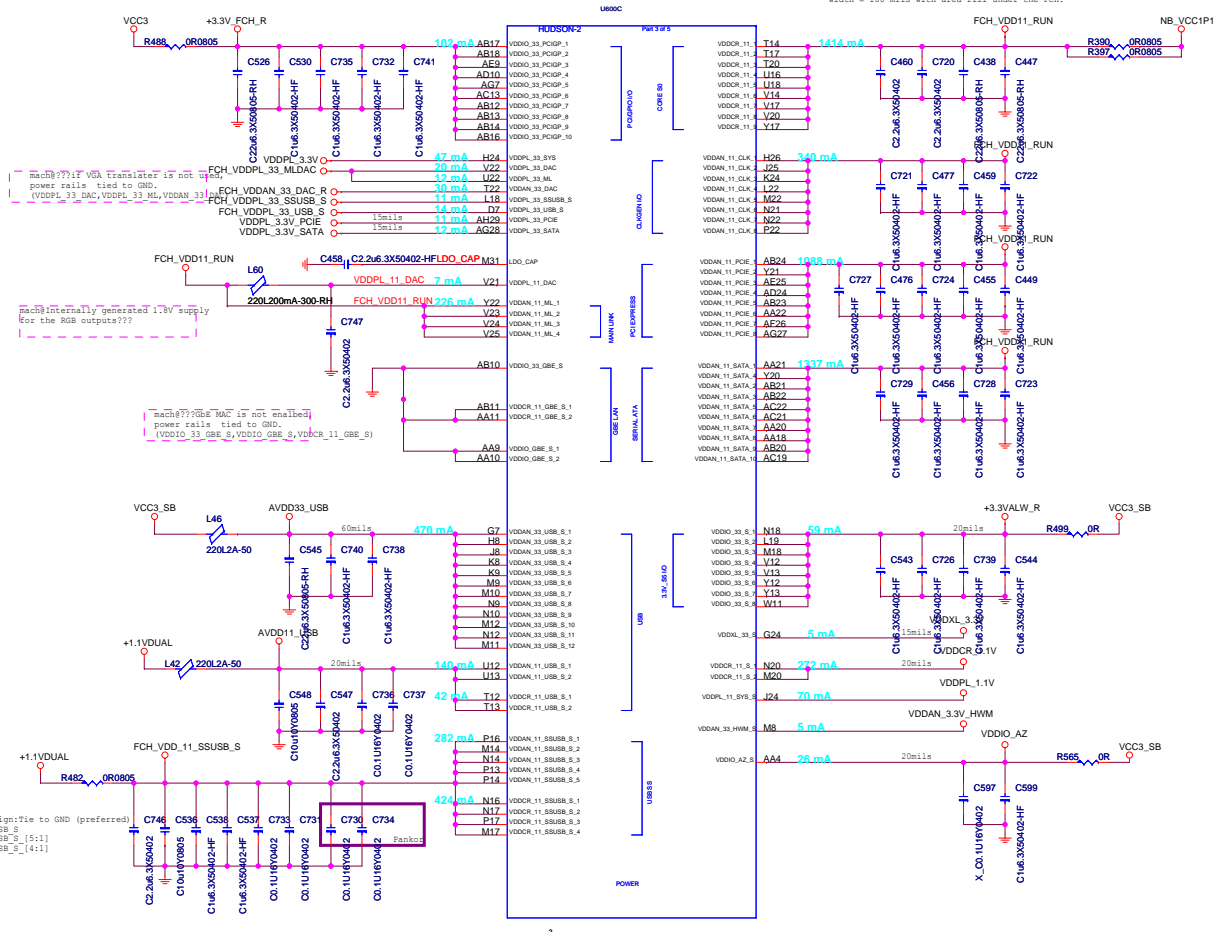
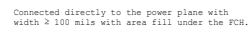
MACH@Reserve OR serial resistors for
SI overshoot/undershoot debug



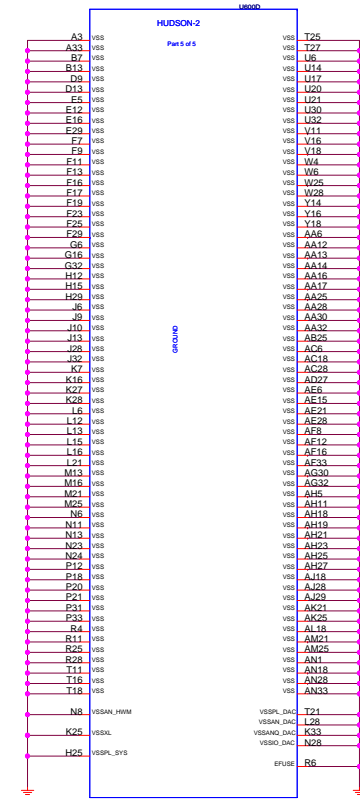
VGA HPD



HUDSON POWER&DECOUPLING

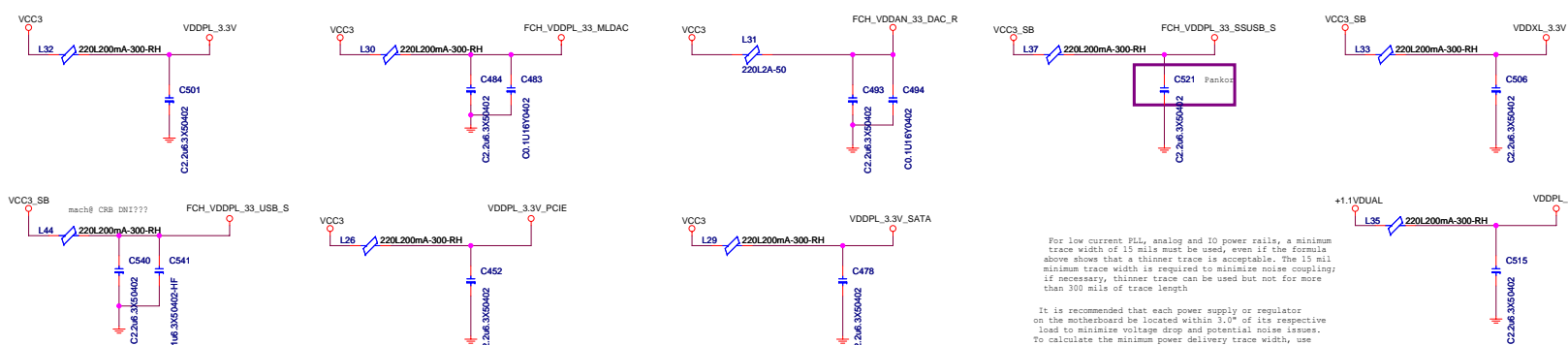


Power Rails	Hudson D3	Hudson D2
NB_VCC1P1	max 4412 mA	
VDDCR_11_[9:1]	1120 mA	1414 mA
VDDAN_11_CLK_[8:1]	340 mA	
VDDAN_11_PCIE_[8:1]	1088 mA	
VDDAN_11_SATA_[10:1]	1337 mA	
VDDAN_11_ML_[4:1]	226 mA	
VDDPL_11_DAC	7 mA	
VCC3	max 319 mA	
VDDIO_33_FCIGF_[10:1]	102 mA	
VDDPL_33_SYS	47 mA	
VDDPL_33_DAC	20 mA	
VDDPL_33_ML	12 mA	
VDDPL_33_PCIE	11 mA	
VDDPL_33_SATA	12 mA	
VDDAN_33_DAC	30 mA	
VCC3_SB	max 659 mA	
VDDIO_33_S_[8:1]	59 mA	
VDDIO_AZ_S	26 mA	
VDDXL_33_S	5 mA	
VDDAN_33_HWM_S	12 mA	
VDDIO_GBE_S[2:1]	145 mA	GND
VDDIO_33_GBE_S	2 mA	GND
VDDPL_33_USB_S	14 mA	
VDDAN_33_USB_S_[12:1]	470 mA	
VDDPL_33_SSUSB_S	11 mA	0 mA
+1.1VDUAL	max 1293 mA	
VDDCR_11_S_[2:1]	272 mA	
VDDCR_11_GBE_S[2:1]	63 mA	GND
VDDPL_11_SYS_S	70 mA	
VDDAN_11_USB_S_[2:1]	140 mA	
VDDCR_11_USB_S_[2:1]	42 mA	
VDDAN_11_SSUSB_S	5282 mA	0 mA
VDDCR_11_SSUSB_S	424 mA	0 mA



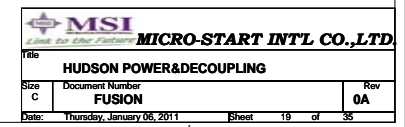
Layout:
VSSPL_SYS;VSSAN_HMM CONNECT TO GND
WITH A SEPRATED VIA

LAYOUT:
ROUTE THE POWER TRACES 15MILS WIDTH AT LEAST
PLACE THE DECOUPLING CAPS CLOSE TO FCH ASAP
PLACE FB<=1" ,CAPS <=0.2"

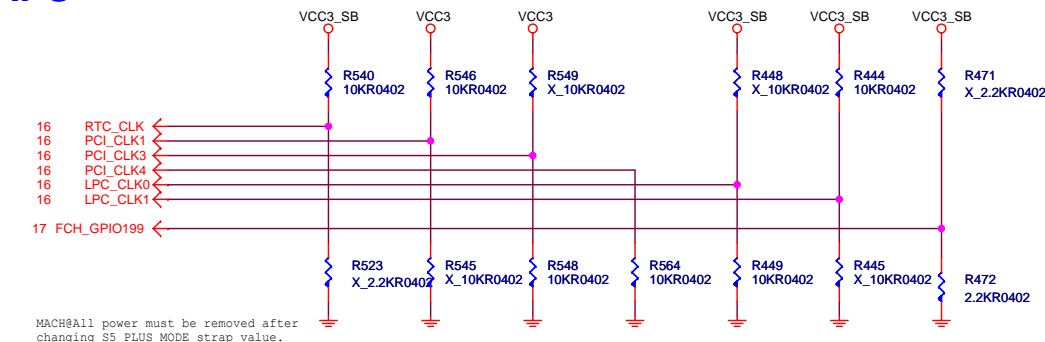


For low current PLL, analog and I/O power rails, a minimum trace width of 15 mils must be used, even if the formula above shows that a thinner trace is acceptable. The 15 mil minimum trace width is required to minimize noise coupling; if necessary, thinner trace can be used but not for more than 300 mils of trace length.

It is recommended that each power supply or regulator on the motherboard be located within 3.0" of its respective load to minimize voltage drop and potential noise issues. To calculate the minimum power delivery trace width, use the formula: $V_{drop} = I \cdot R$, where $R = \rho \cdot L / A$ (ρ = resistivity of material, L = trace length, A = trace cross-sectional area). V_{drop} must be $< 2.5\%$ of the nominal power rail voltage under maximum current conditions



FCH REQUIRED STRAPS



	RTCCLK	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO199
PULL HIGH	S5 PLUS MODE DISABLED DEFAULT	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	Reserved	EC ENABLED	INTERNAL CLOCK GEN ENABLED DEFAULT	LPC ROM
PULL LOW	S5 PLUS MODE ENABLED	FORCE PCIE GEN1	IGNORE DEBUG STRAPS DEFAULT	Required setting for intergrated CLOCK MODE DEFAULT	EC DISABLED DEFAULT	INTERNAL CLOCK GEN DISABLED	SPI ROM DEFAULT

FCH DEBUG STRAPS

Provided test point access for lab use.
FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

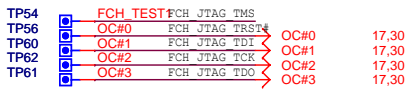


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	RESERVED	Normal REFCLK Termination DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL DOWN	BYPASS PCI PLL	RESERVED	Inverted REFCLK Termination	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

FCH PCIE EEPROM STRAPS



FCH ICE DEBUG /JTAG TEST PINS

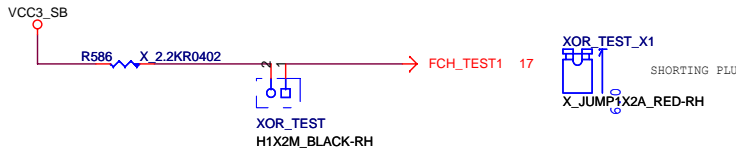



FCH XOR CHAIN TEST



TP55	FCH_TEST0	FCH_TEST0	17
TP58	FCH_TEST2	FCH_TEST2	17

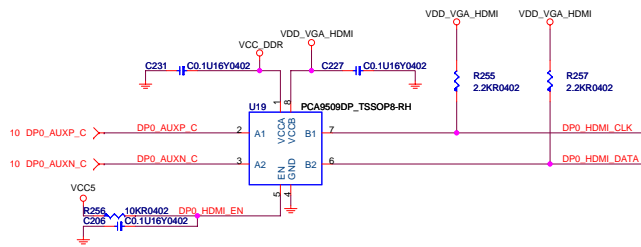
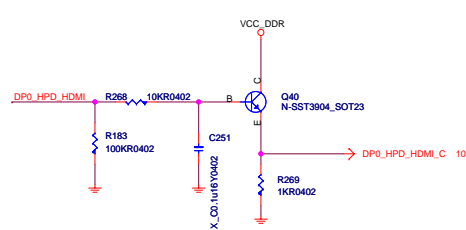
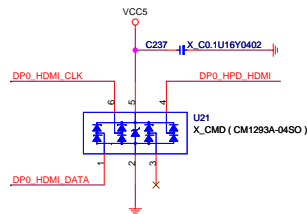
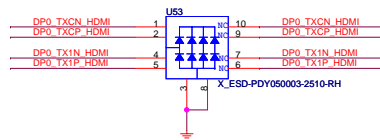
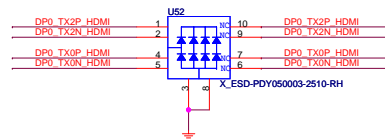
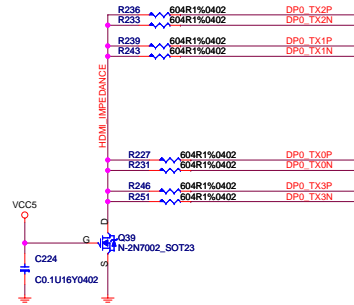
FEST2	FEST1	FEST0	Description
0	1	X	Enable test mode



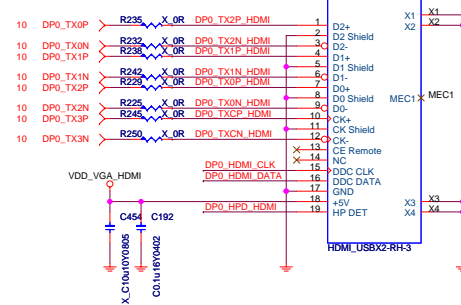
**MICRO-START INT'L CO.,LTD.**

Title HUDSON STRAPS		
Size B	Document Number FUSION	Rev 0A
Date: Thursday, January 06, 2011	Sheet 20	of 35

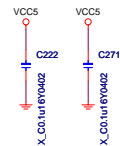
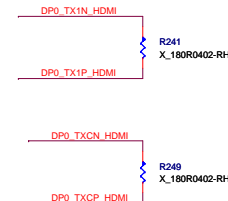
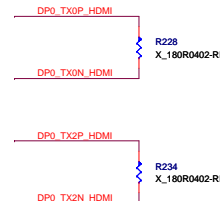
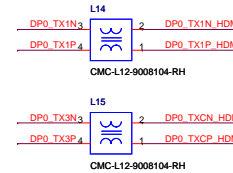
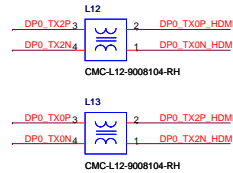
HDMI CONN,



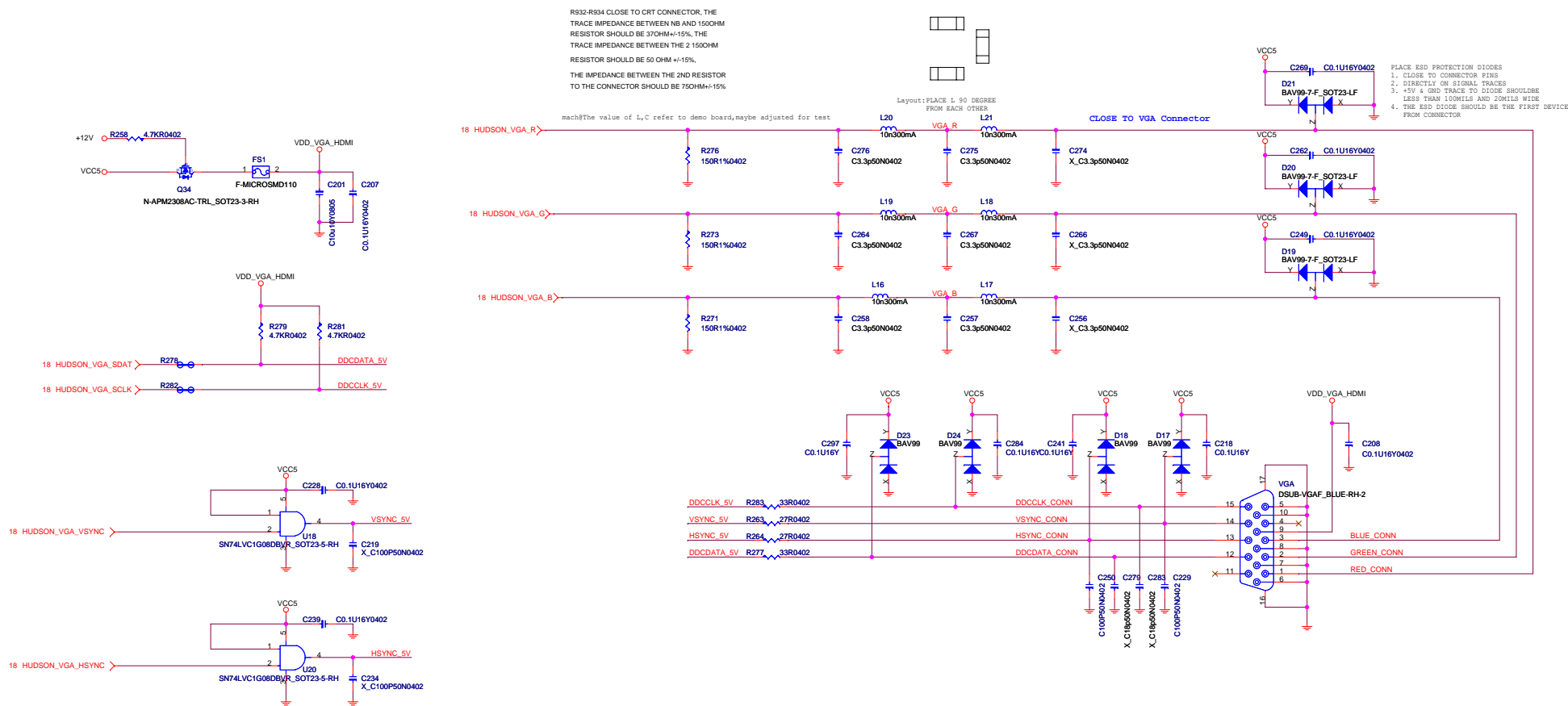
DP CONFIGURATION TABLE					
INTERFACE	DP PORT OF PM1				
DP	3	2	1	0	
HDMI	Channel1	Channel2	Channel3	Channel4	



L12-9008054-M09/L12-9008044-T34/L12-9008054-M09

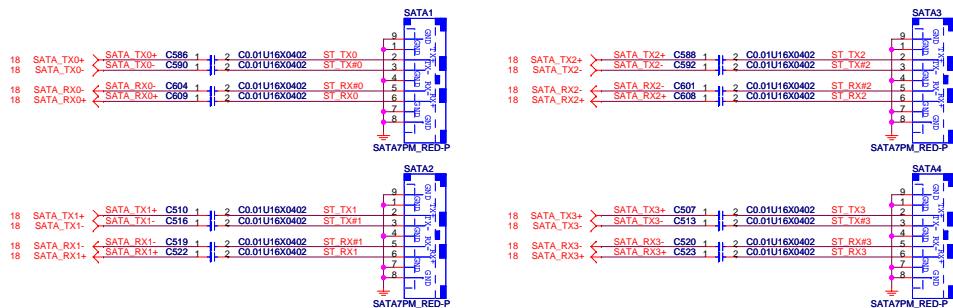


VGA CONNECTOR

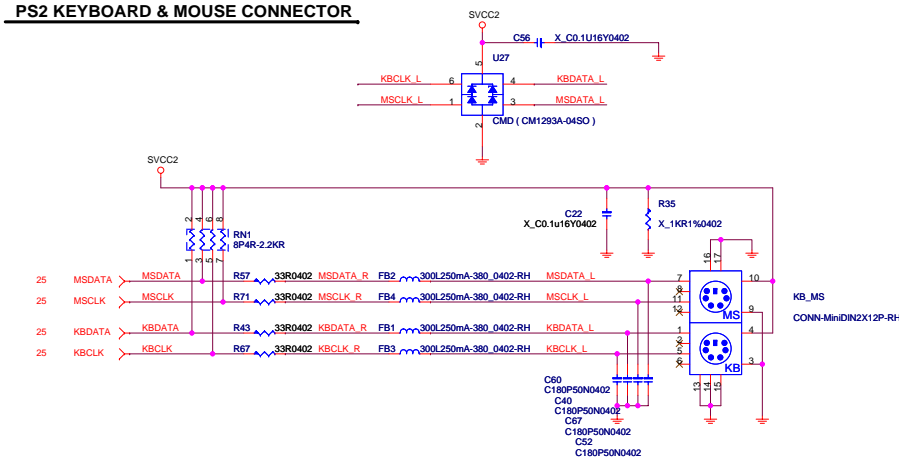


Multiple eSATA function

Layout: For Gen 3.0, trace length within 3''

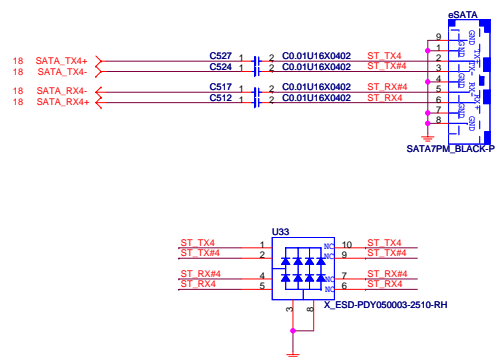


PS2 KEYBOARD & MOUSE CONNECTOR



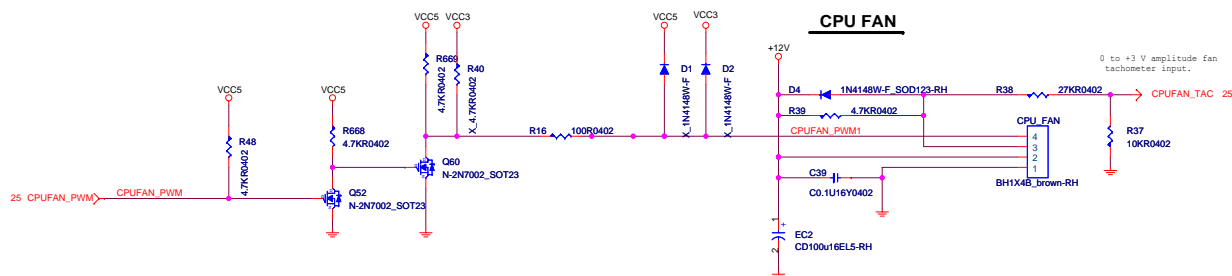
eSATA Conn. WO re-driver

Layout: For onboard eSATA conn. without redriver IC, trace length within 6"

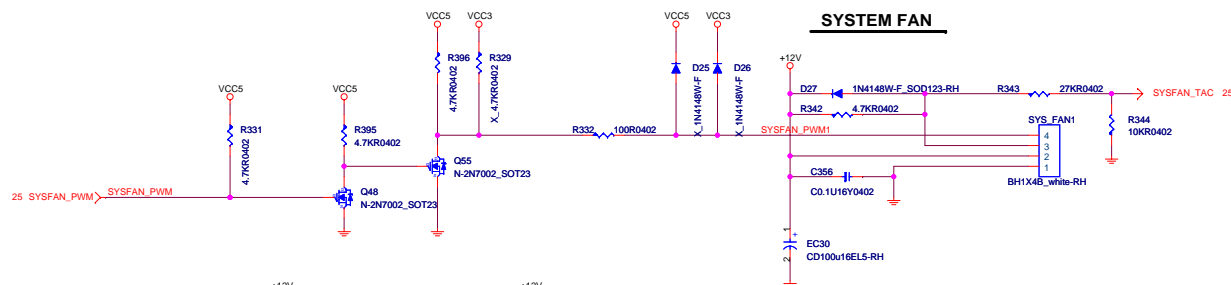


PWM FAN CONTROL

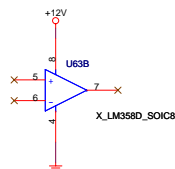
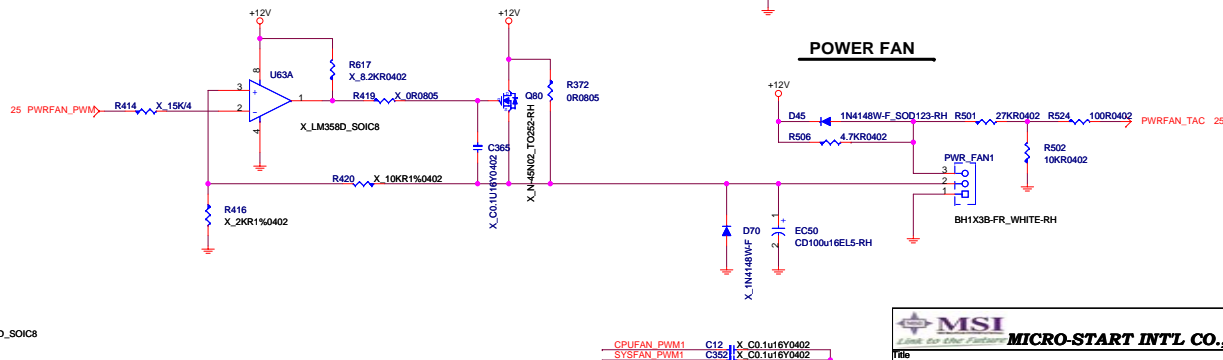
CPU FAN



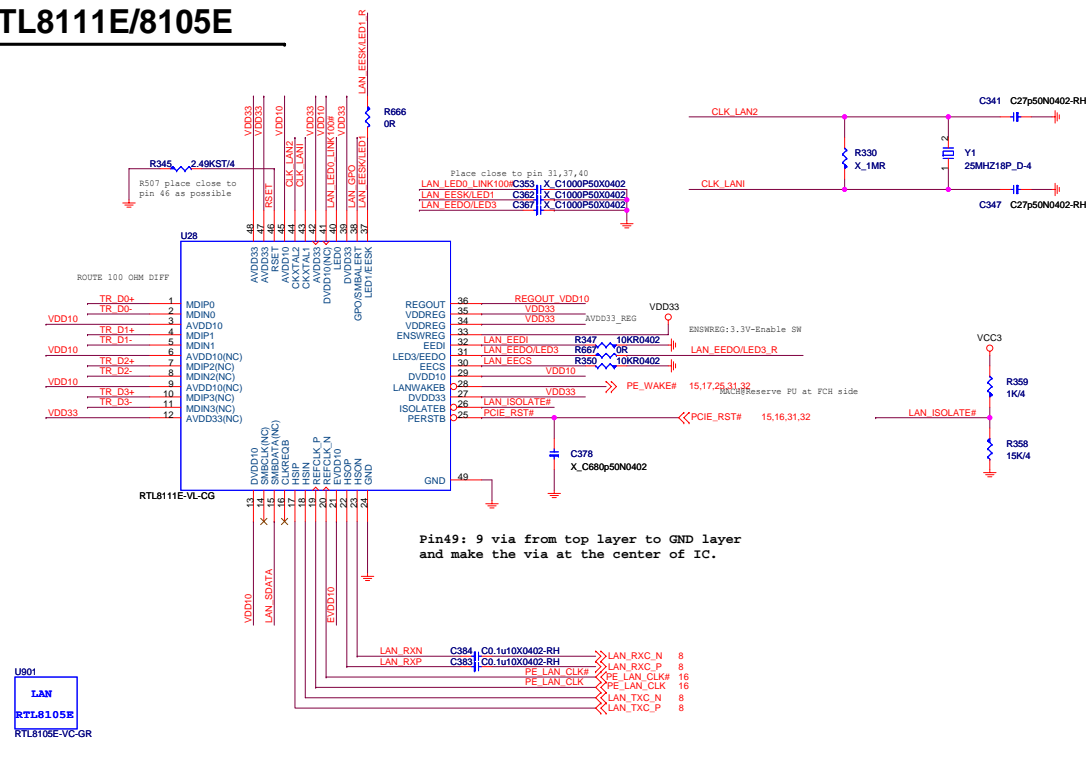
SYSTEM FAN



POWER FAN

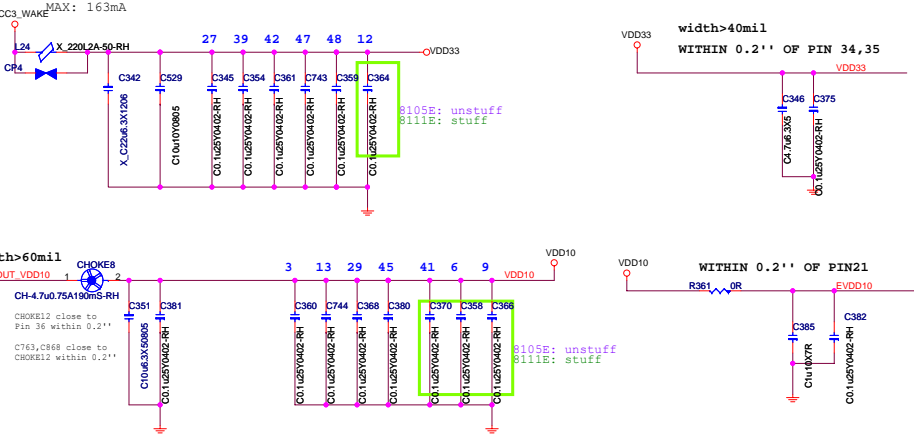


RTL8111E/8105E



Pin49: 9 via from top layer to GND layer
and make the via at the center of IC.

3.3v Power on rise time : 1~100ms.



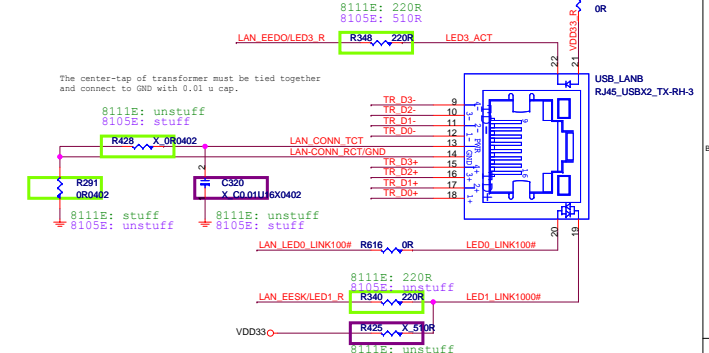
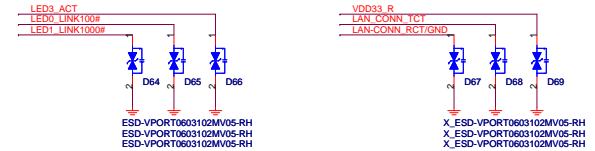
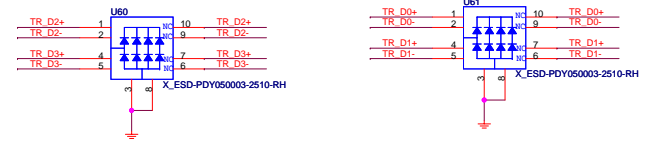
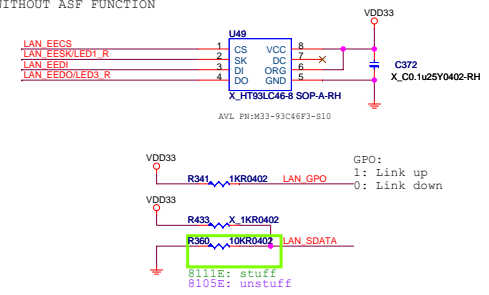
8105E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

USE Efuse/BIOS PATCH WITHOUT ASF FUNCTION



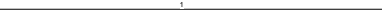
The center-tap of transformer must be tied together and connect to GND with 0.01 u cap.

N58-22F0851-F02/N58-22F0851-I60 30u

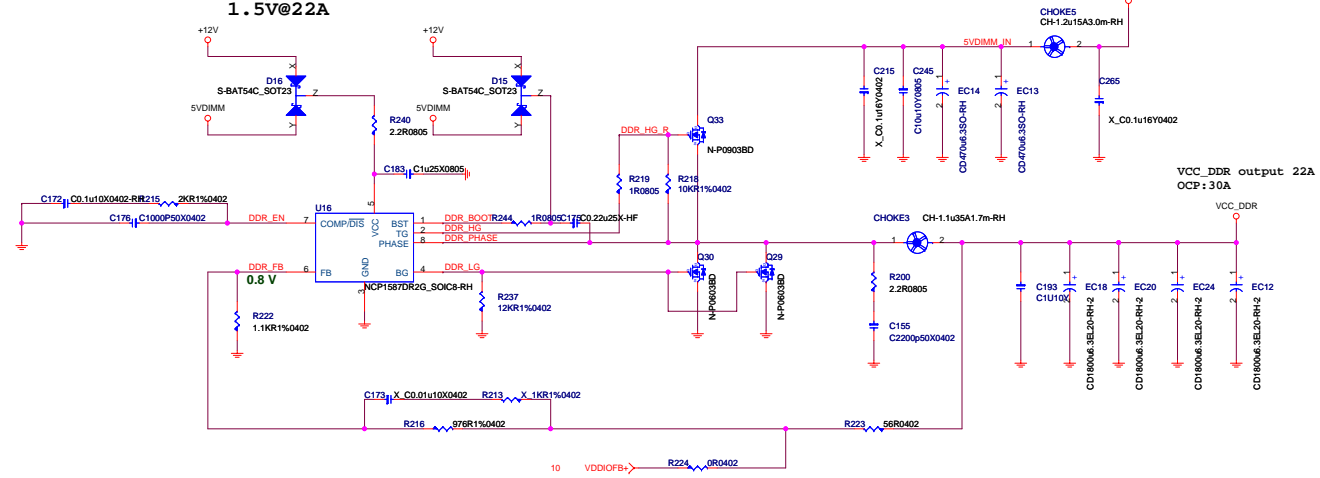
only support LED0+LED1/LED1+LED3 dual color LED combinations when using EEPROM



LAN-RTL8111E/8105E.			
Size C	Document Number FUSION		Rev 0A
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DDR III 1.5V POWER
1.5V@22A

[illegible]

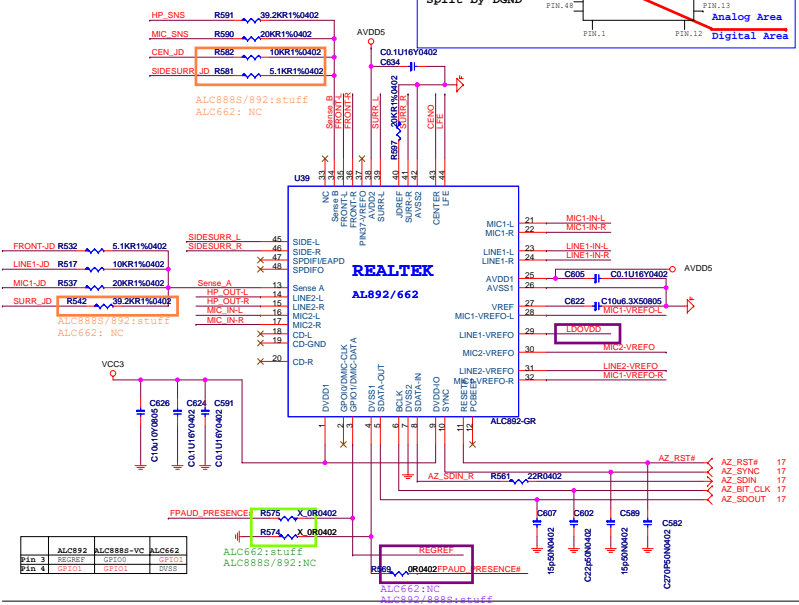
CPU_VDDP POWER 1.2 V@5A

CPU_VDDR POWER 1.2 V@5A

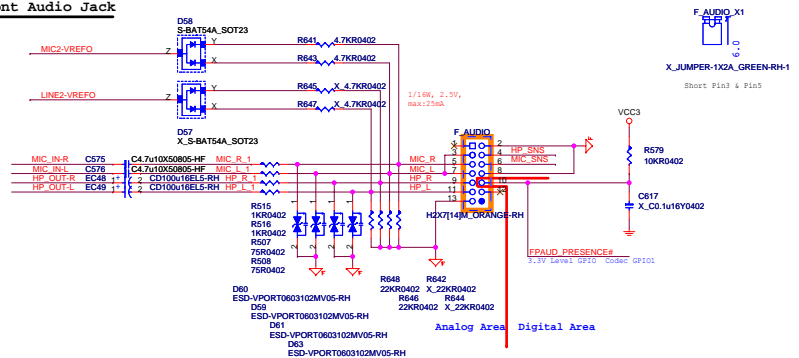
[illegible]

Default is ALC892

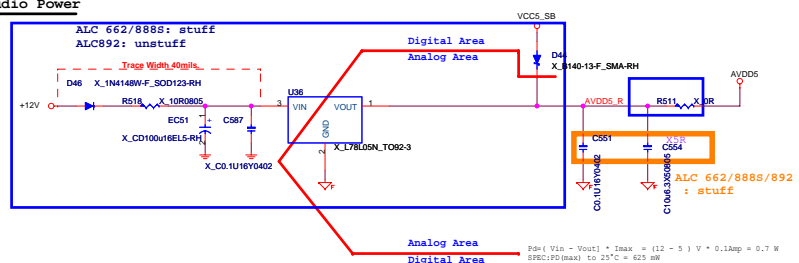
JD resistors should be placed
as close as possible to the
sense pin of CODEC.



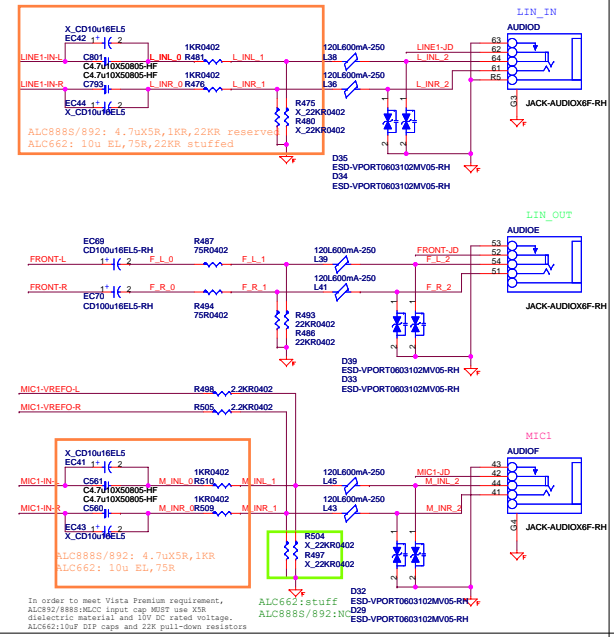
Front Audio Jack



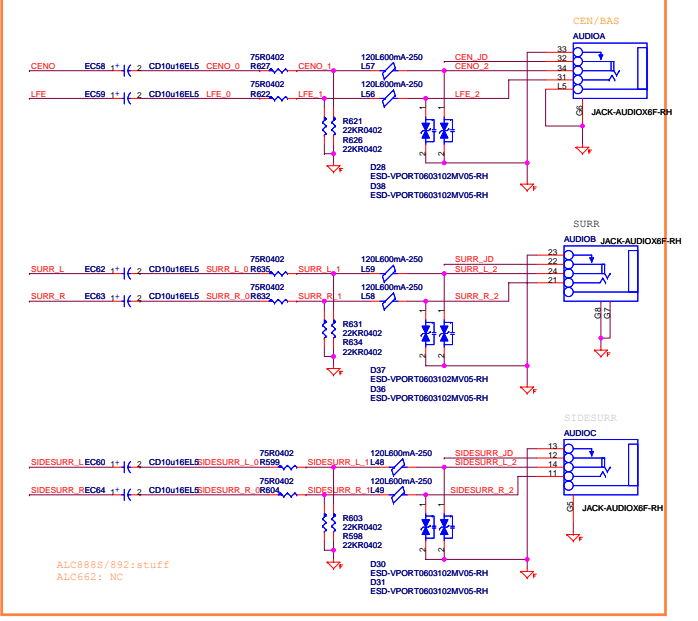
Audio Power



Rear Phone Jack 3 IN 1

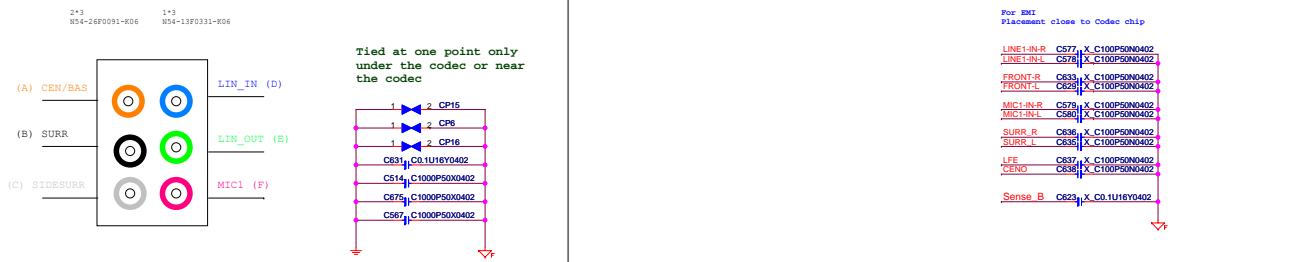


Rear Phone Jack 6 IN 1



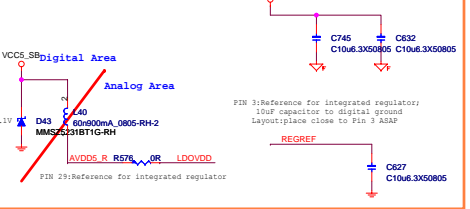
EMI

For EMI



ALC892 PART

```
ALC662/88S:NC
ALC892:stuff
```



662: 5V: 37mA (PIN25, 38)
3V: TBDmA

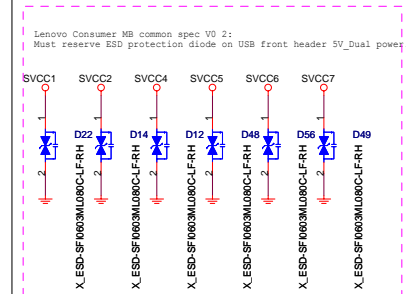
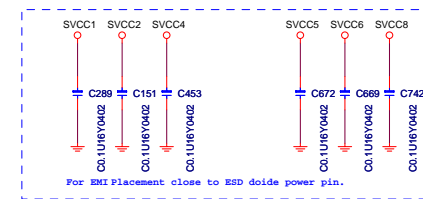
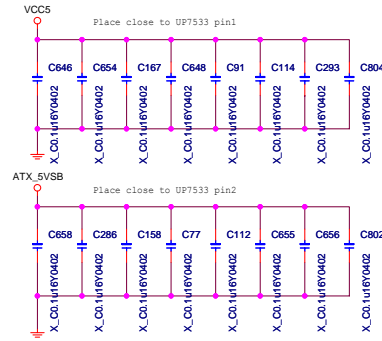
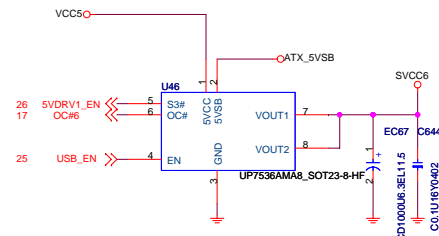
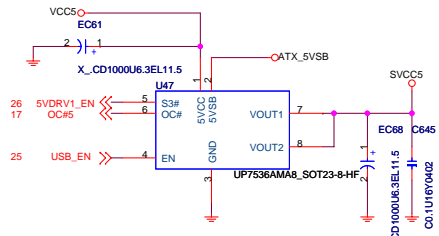
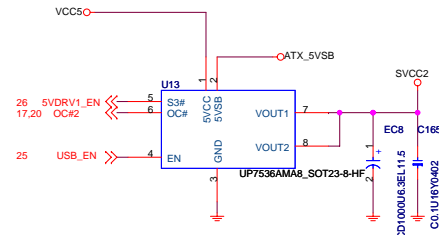
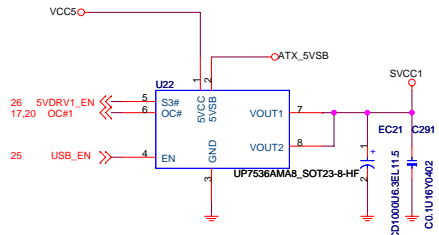
888S: 5V: 61mA (PIN25, 38)
3V: 41mA

892: 5V: 45.8mA (PIN29)
3V: 11mA

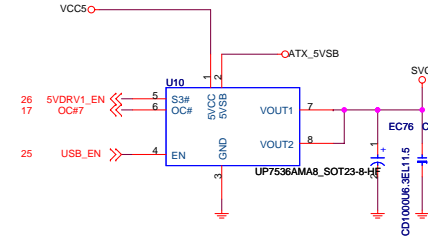
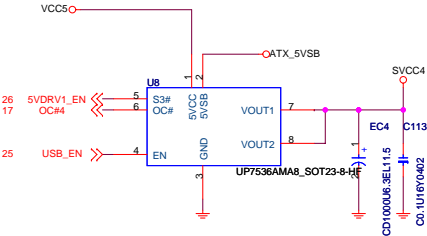
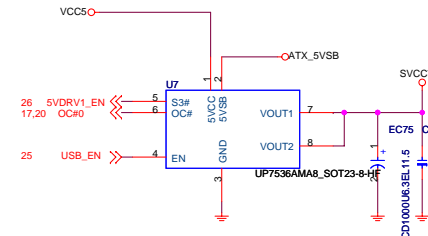
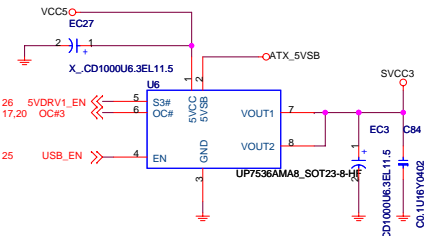
```
USB 3.0 trace length
Front pin header within 3.5''
```

Title			USB POWER/CONNECTORS		
Size	Document Number				Rev
Custom	FUSION				0A
Date:	Thursday, January 06, 2011		Sheet	29	of 35

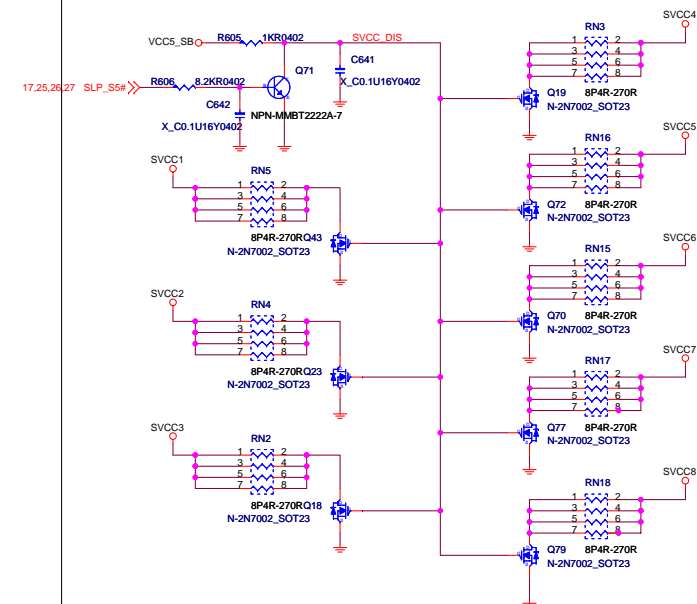
USB 2.0 0.5A pert port



USB 3.0 0.9A pert port



USB power discharge circuit



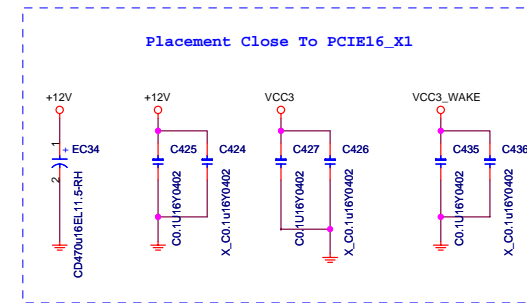
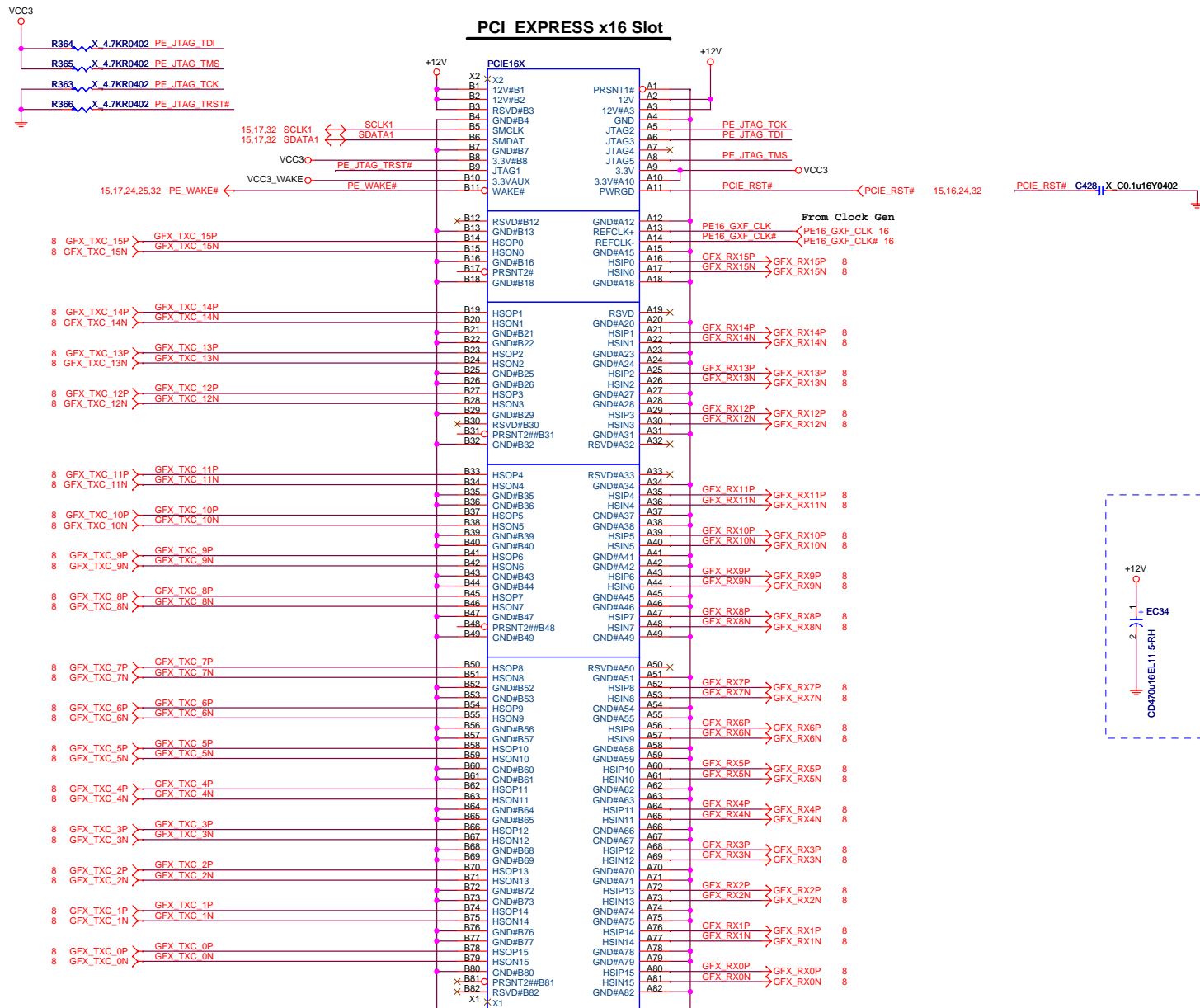
Use low-pass filter to prevent glitches during plug/unplug events.

OC#0 C111 C0.1U16V0402
OC#1 C96 C0.1U16V0402
OC#2 C116 C0.1U16V0402
OC#3 C132 C0.1U16V0402
OC#4 C141 C0.1U16V0402
OC#5 C603 C0.1U16V0402
OC#6 C748 C0.1U16V0402
OC#7 C749 C0.1U16V0402

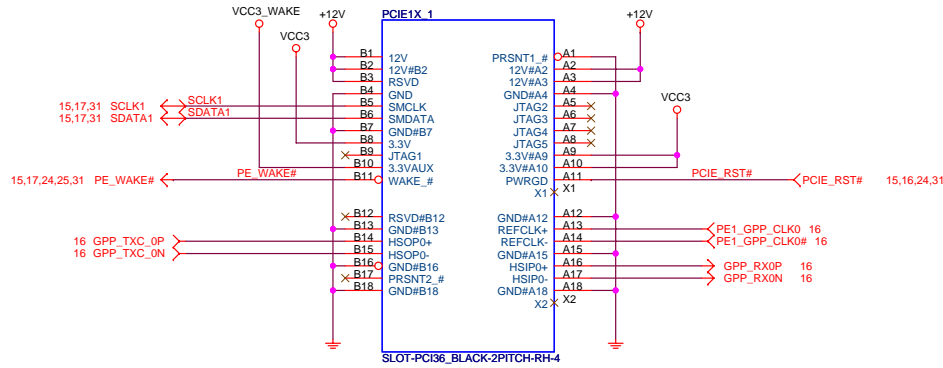


USB POWER/DISCHARGE			
Size	Document Number	FUSION	Rev
Custom			0A
Date:	Thursday, January 05, 2011	Sheet	30 of 35

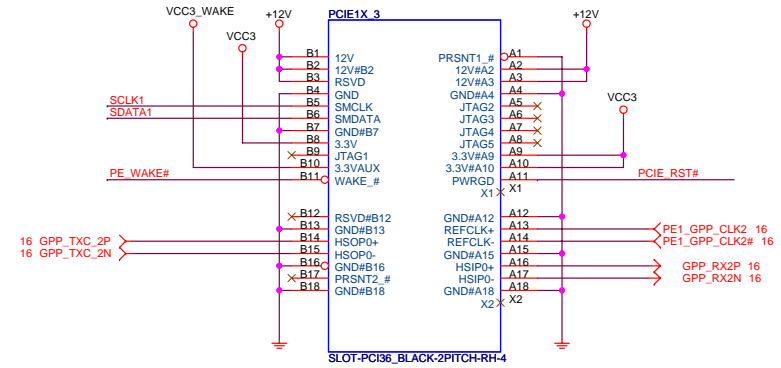
PCI Express Slot x16



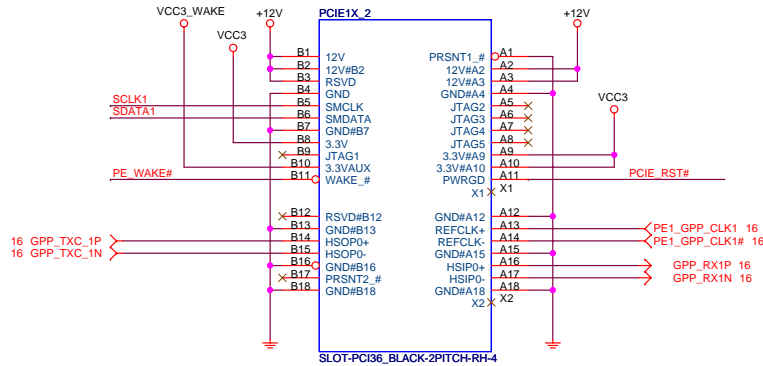
PCI EXPRESS X1 Slot-1



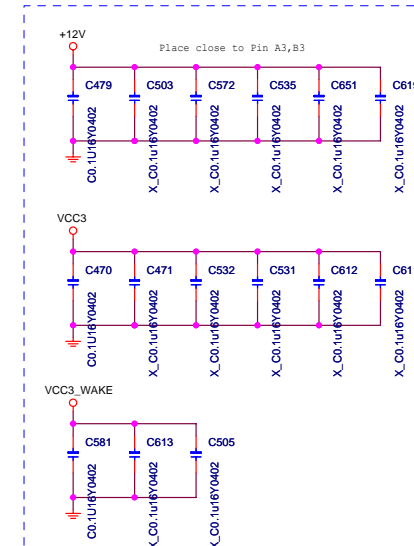
PCI EXPRESS X1 Slot-3



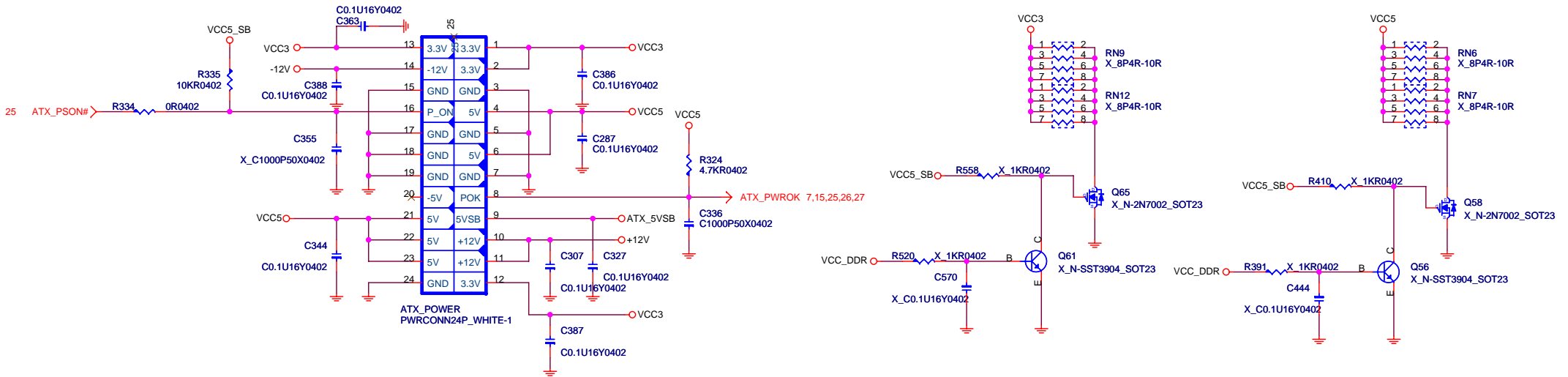
PCI EXPRESS X1 Slot-2



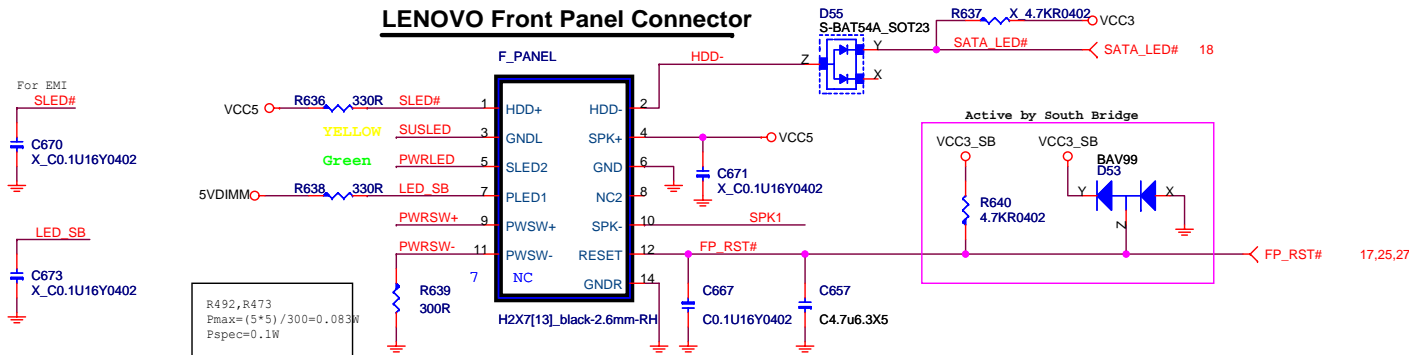
PCIE_RST# C472 X_C0.1u16Y0402



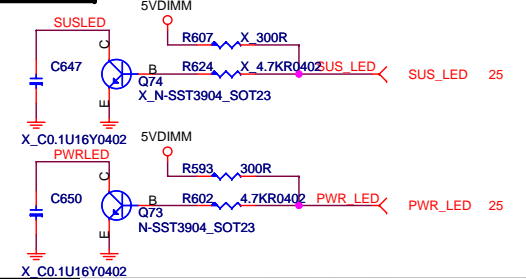
ATX CONNECTOR



LENOVO Front Panel Connector



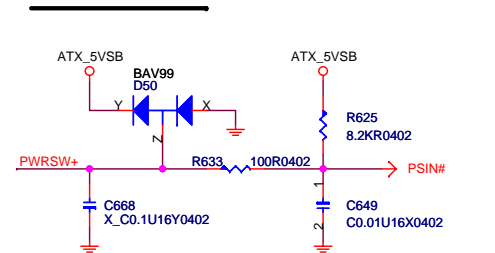
POWER LED



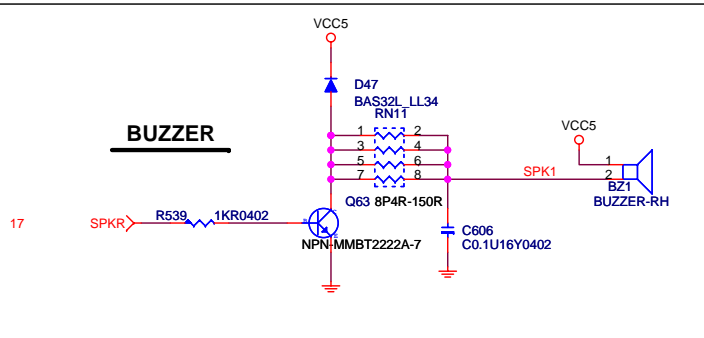
power LED definition

HD (IDE Hard Disk Active LED)	
Pin 1: LED anode(+)	Pin 8: LED cathode(-)
(Power LED)	Pin 3: LED cathode(-) (green)
Power Switch	Pin 2: LED cathode(-) (yellow)
LED Status (Dual color LED)	Open/Normal Operation
System State	Close: Power on / Off
S0	Dual Color POWER LED State
S1	Steady Green
S3	Green Blinking (frequency is under 1Hz)
S4/S5	Steady Yellow
Default S5 in lose power	Off
Note series resistor is 330Ω	

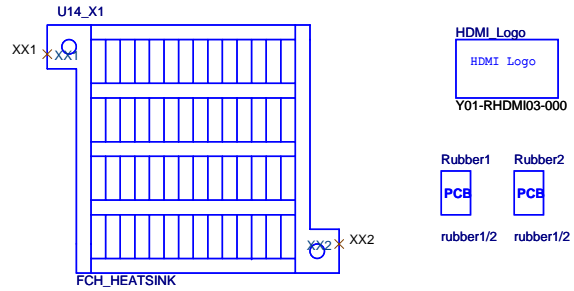
POWER BUTTON



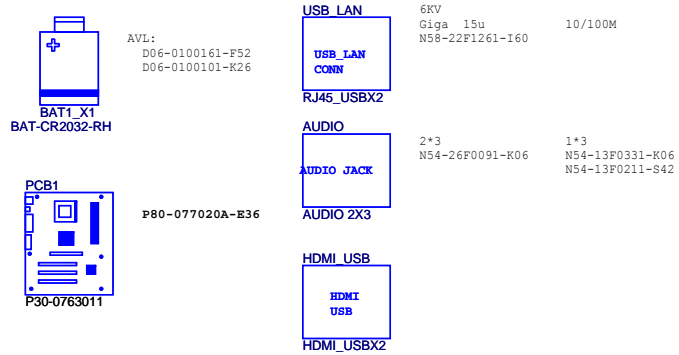
BUZZER



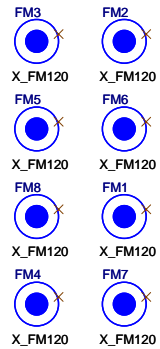
HEAT SINK



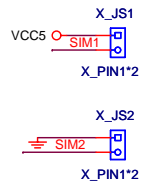
MANUAL PART



Optics Orientation Holes



Simulation



Pangkor

